

PCB NO : DAA000OK011  
BOM P/N : 451AP931L01

ZZZ



PCB 36N LA-K662P REV1 M/B GOLD A31 I  
DAA000OK011  
PCB@

# Compal Confidential

## CML-H MB Schematic Document

Rev: 1.0

2020.12.29

@ : Un-pop Component  
JP@/PJP@ : JUMP  
5VFAN@/12VFAN@ : JUMP for FAN power

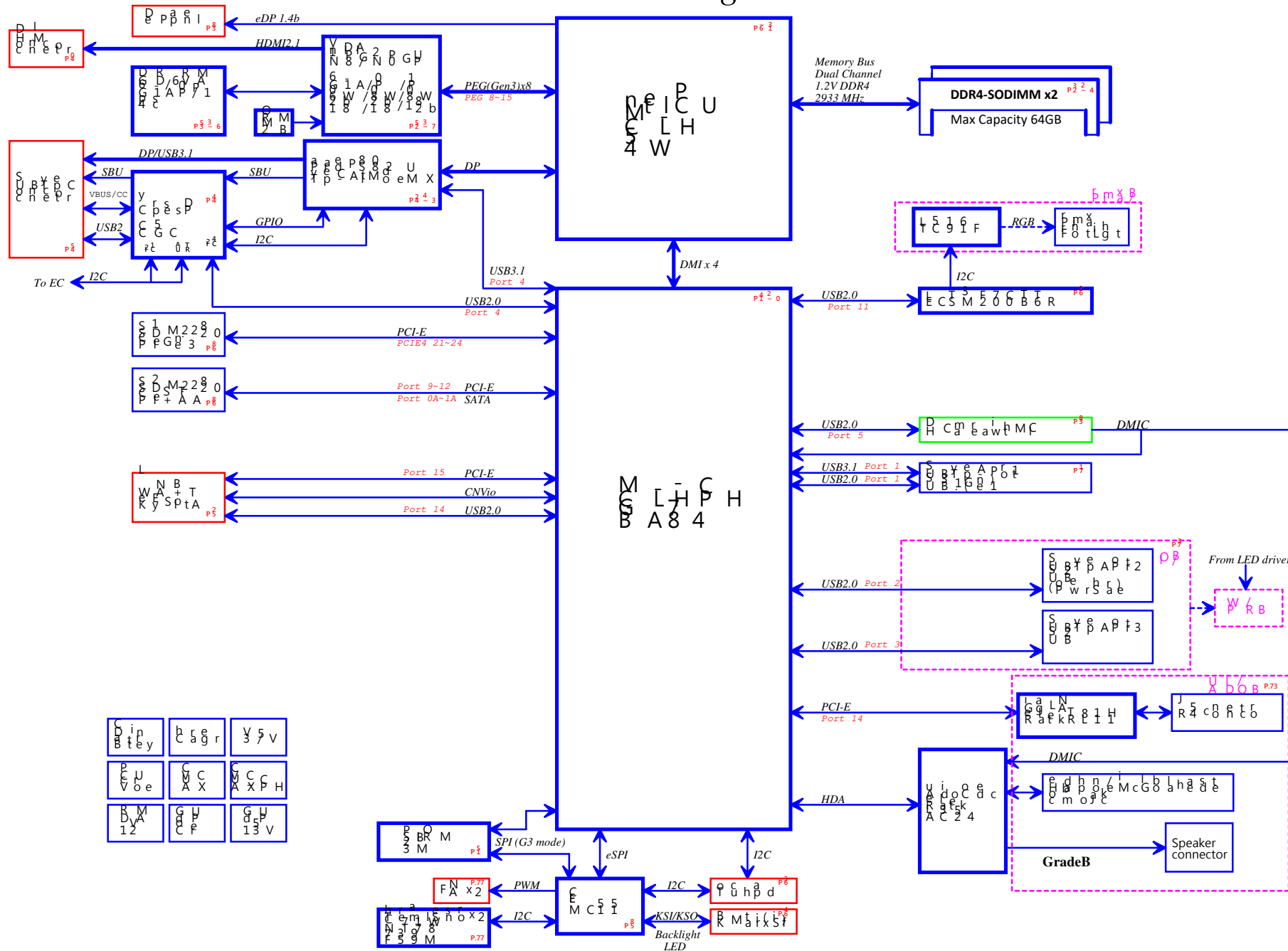
EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
GN20P\_ESD@/GN20P\_EMI@ : EMI and ESD Component for GN20P GPU only  
XDP@ : XDP Component  
CONN@ : Connector Component  
SW@ : Debug PWR Button

CNV@/@CNV@ : CNVi Support  
G3@ : EC G3 Flash Sharing

N18P@/GN20P@:GPU Support  
45492@/45495@: OVR-M Support

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### Block Diagram



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Board ID table

Item	Pull-down	Pull-up	Voltage	Board ID/Model ID
1	100	10K	3.000	Pre-EVT
2	100	17.8K	2.801	EVT
3	100	27K	2.598	DVT1
4	100	37.4K	2.402	DVT2
5	100	49.9K	2.201	Pilot
6	100	64.9K	2.001	
7	100	82.5K	1.808	
8	100	107K	1.594	
9	100	154K	1.299	
10	100	200K	1.1	

Power State

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Port	Power Rail	Device	Address
PCH_SMBCLK PCH_SMBDATA	+3VALW_PCH	JDIMM1	
		JDIMM2	

EC SMBUS Address Table


EC_SMBUS Port	Power Rail	Device	Address
GPU_THM_SMBCLK GPU_THM_SMBDAT	+3VS	Thermal 1	0x98h
		Thermal 2	0x9Ah
		GPU (GN20E)	0x9E
PBAT_CHG_SMBCLK PBAT_CHG_SMBDAT	+3VALW_EC	BAT	0x16
		CHGR	0x12
DAT_TP_SIO_I2C_CLK CLK_TP_SIO_I2C_DAT	+TP_VDD	Touch Pad	0x2C
UPD1_SMBCLK UPD1_SMBDAT	+3V_VSYS	CCG5C	0x08


CML-H-PCH HM470

HSIO	USB3.2	PCIe	SATA3	Function
0	1			JUSB
1	2			
2	3			
3	4			CPU side Type C
4	5			
5	6			
6	7			
7	8			
8				
9				
10				
11				
12		7		
13				
14		9		
15		10		JSSD2 , 2280 SATA x2 / PCIe x4
16		11	0A	
17		12	1A	
18		13	0B	
19		14	1B	LAN
20		15		WLAN
21		16		
22		17		
23		18		
24		19		
25		20		
26		21		
27		22		JSSD1 , 2280 PCIe x4
28		23		
29		24		

USB2	Function
1	JUSB
2	JUSB
3	JUSB
4	CPU side Type C
5	HD CAM
6	
7	
8	
9	
10	
11	ELC MCU
12	
13	
14	Bluetooth

Symbol Note :

 Digital Ground

 Analog Ground

60 mils/1A = 1/3 oz  
40 mils/1A = 0.5 oz  
20 mils/1A = 1 oz  
10 mils/1A = 2 oz

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Processor core rail	ON	OFF	OFF	OFF	OFF
+VCCGT	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+VCCSA	System Agent power rail	ON	OFF	OFF	OFF	OFF
+VCCIO	IO power rail	ON	OFF	OFF	OFF	OFF
+3.3V_BAT_LDO	RTC power	ON	ON	ON	ON	ON
+RTC_CELL	+3.3V_BAT_LDO/+3VLP for suspend power	ON	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW_PCH	+3VALW Primary Power Well for PCH	ON	ON	ON	ON*	OFF
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1VALW	System +1.05V power rail	ON	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail (VDDQ)	ON	ON	ON	OFF	ON
+0.6V_DDR_VTT	DDR4 +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail (Vpp)	ON	ON	ON	OFF	ON
+VCCST	Sustain voltage for processor in Standby modes	ON	ON	ON	OFF	OFF
+VCCSTG	Gated version of VCCST	ON	OFF	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

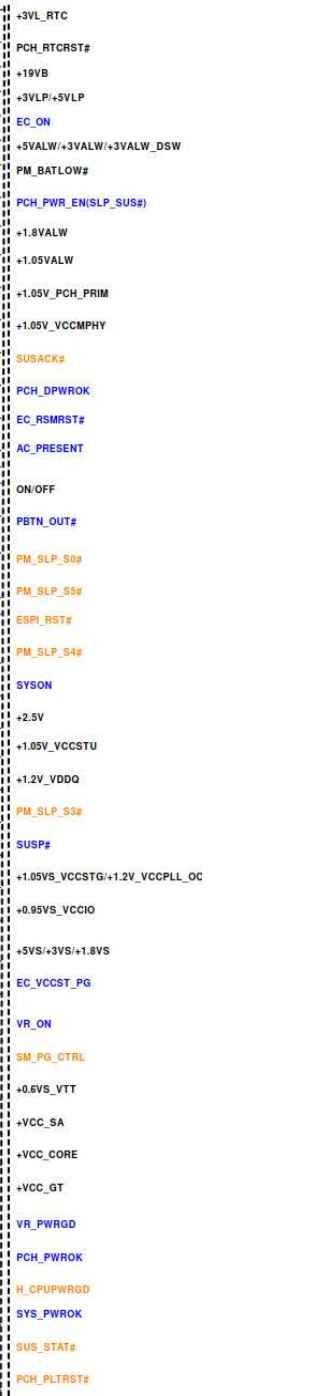
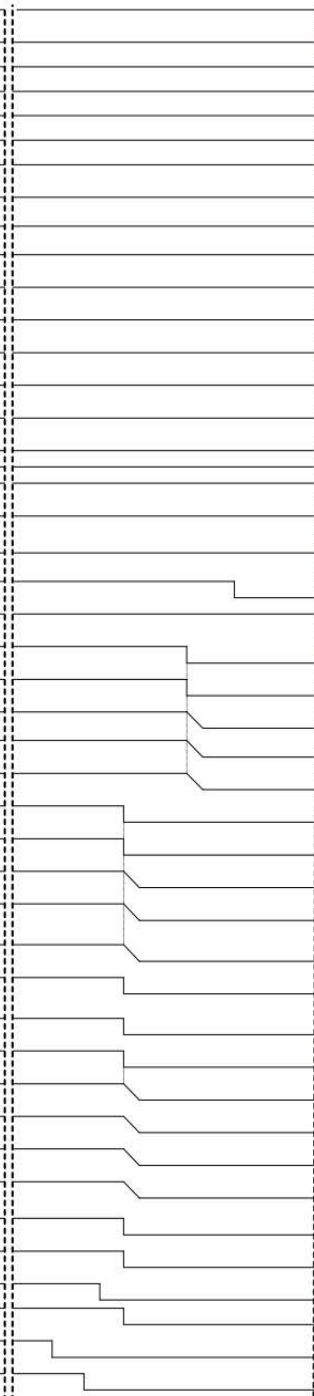
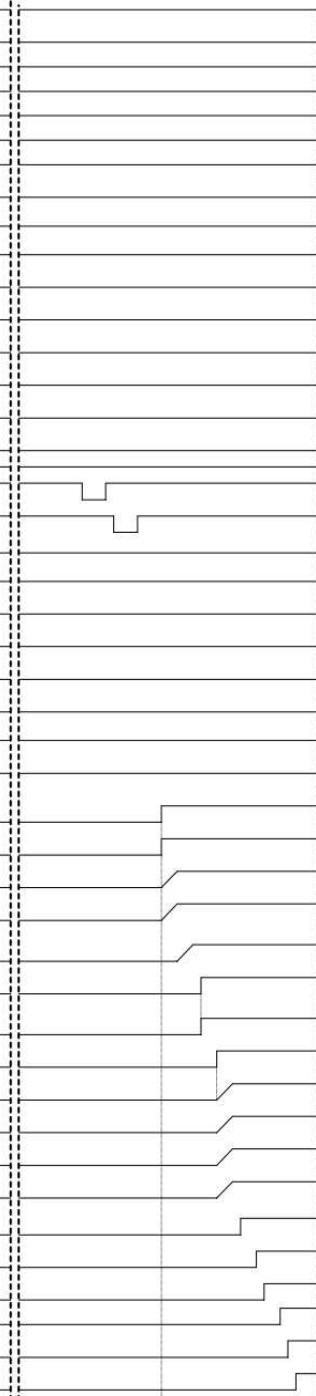
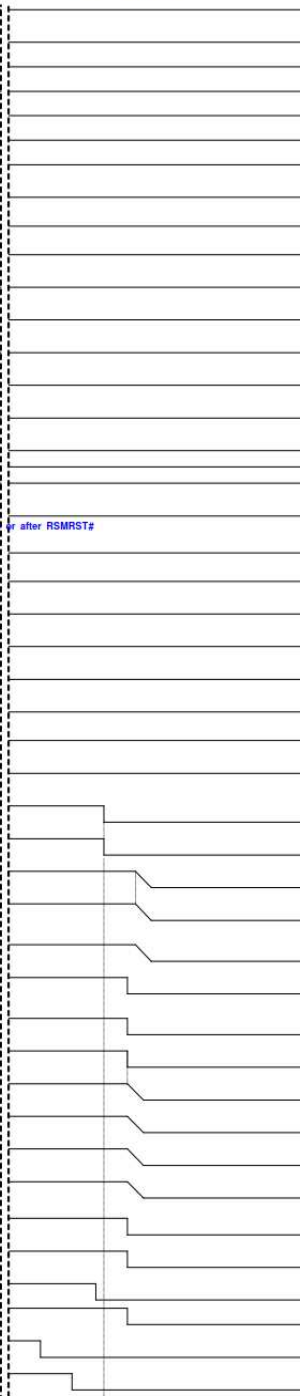
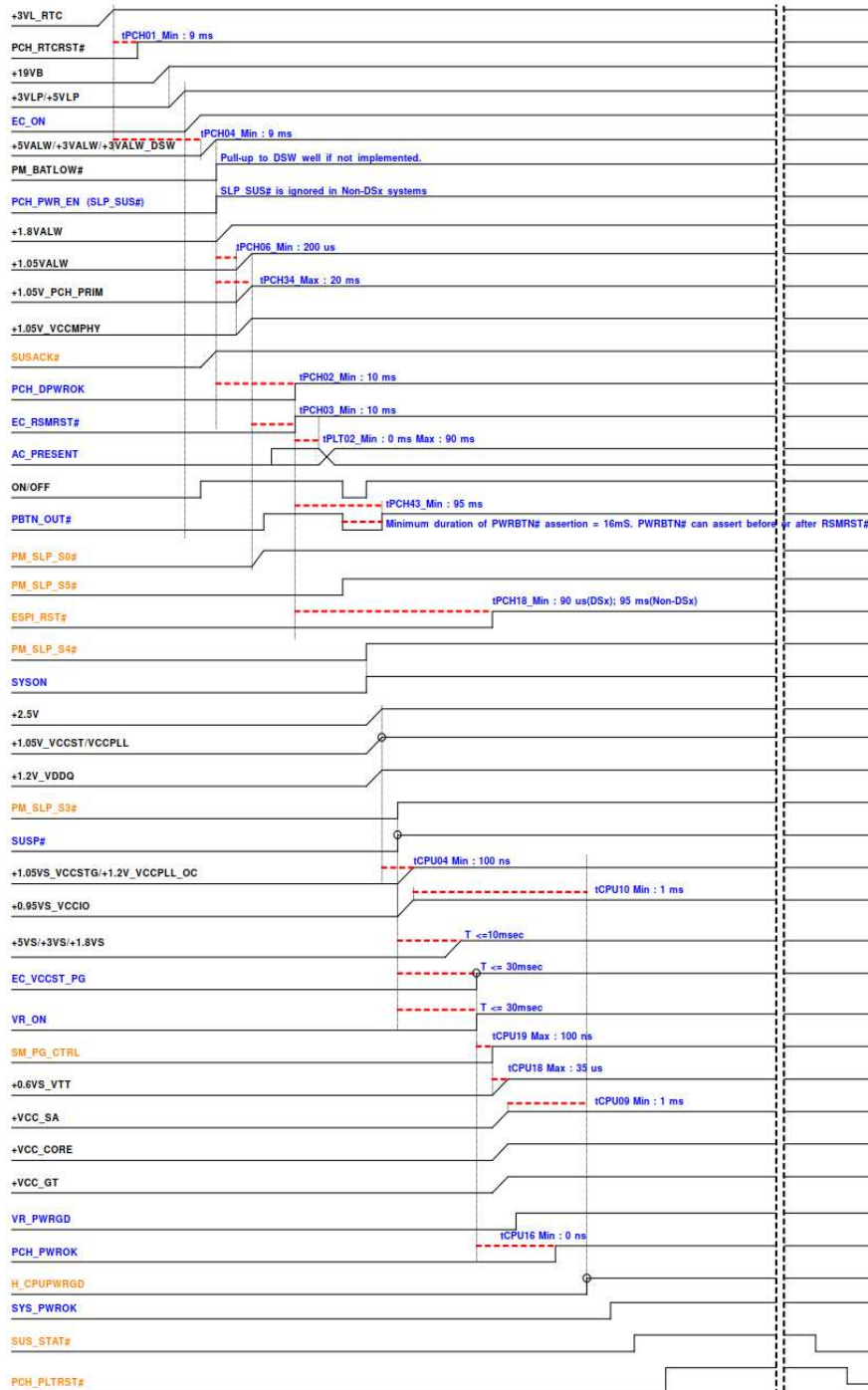


G3-&gt;S0

S0-&gt;S3

S3 -&gt;S0

S0-&gt;S5



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## CPU R1:

UC1

**CPU I5 QS**

CL8070104441108 QVW4 R1 2.4G S  
SA0000DW10L  
QVW4R3@

UC1

**CPU I7 QS**

CL8070104399317 QVW6 R1 2.2G S  
SA0000DW20L  
QVW6R3@

## CPU R3:

UC1

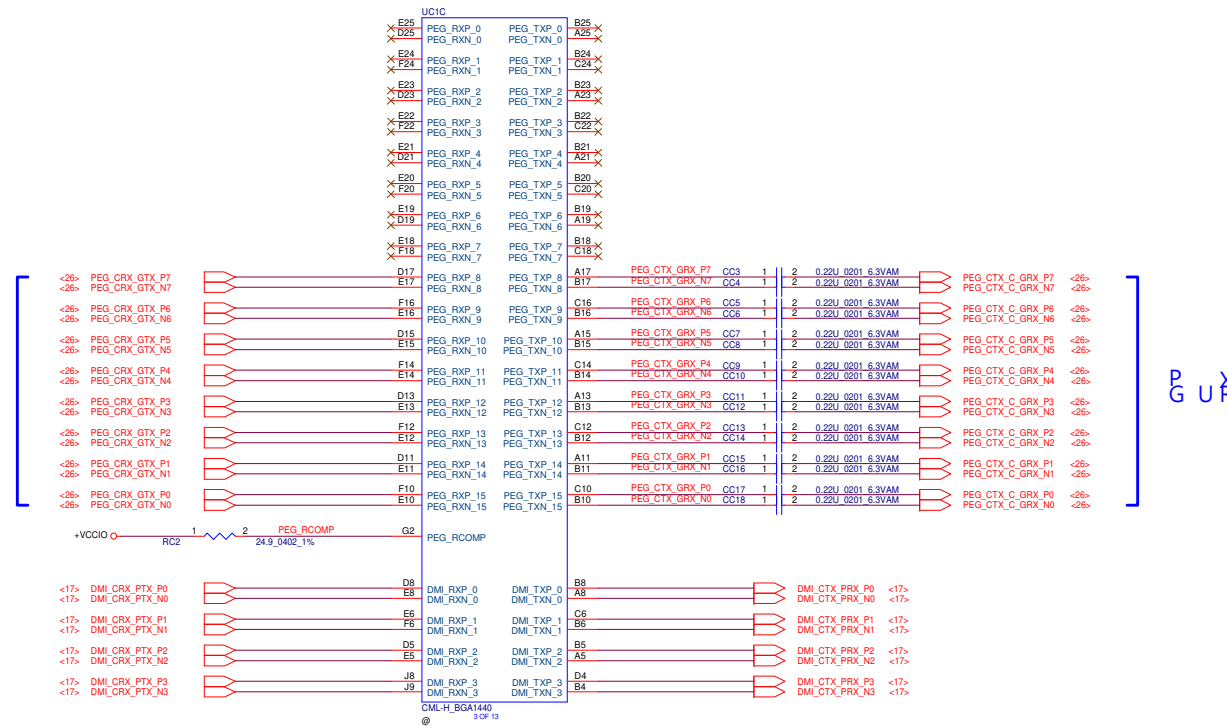
**CPU I5 MP**

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SA0000DW12L  
SRK3XR3@

UC1

**CPU I7 MP**

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SA0000DW22L  
SRK3YR3@



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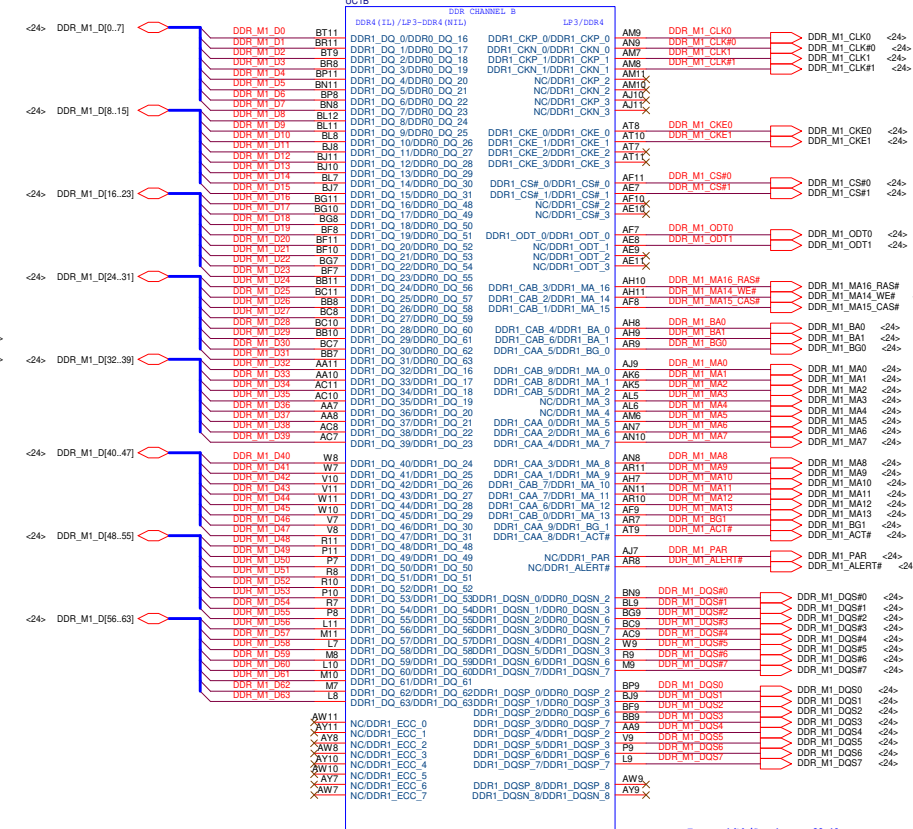
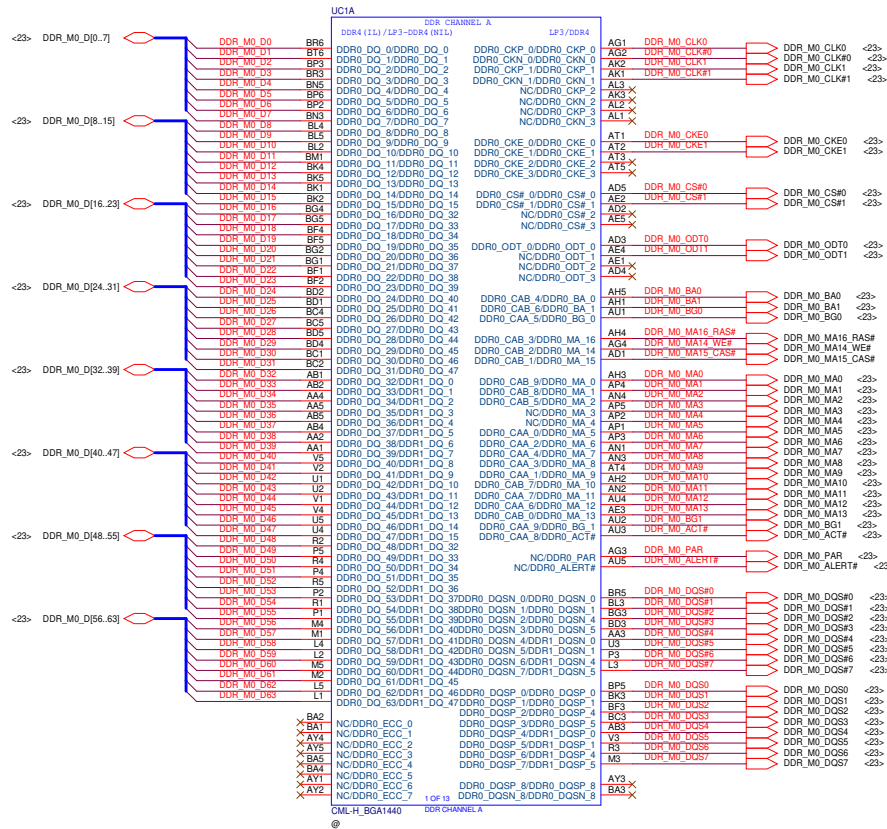
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# Reserve

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## CHANNEL-A

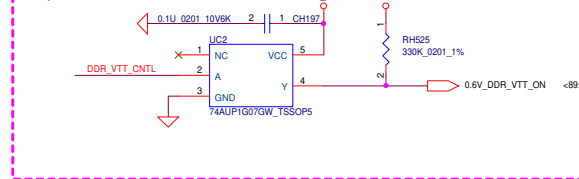
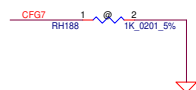
### Interleaved Memory

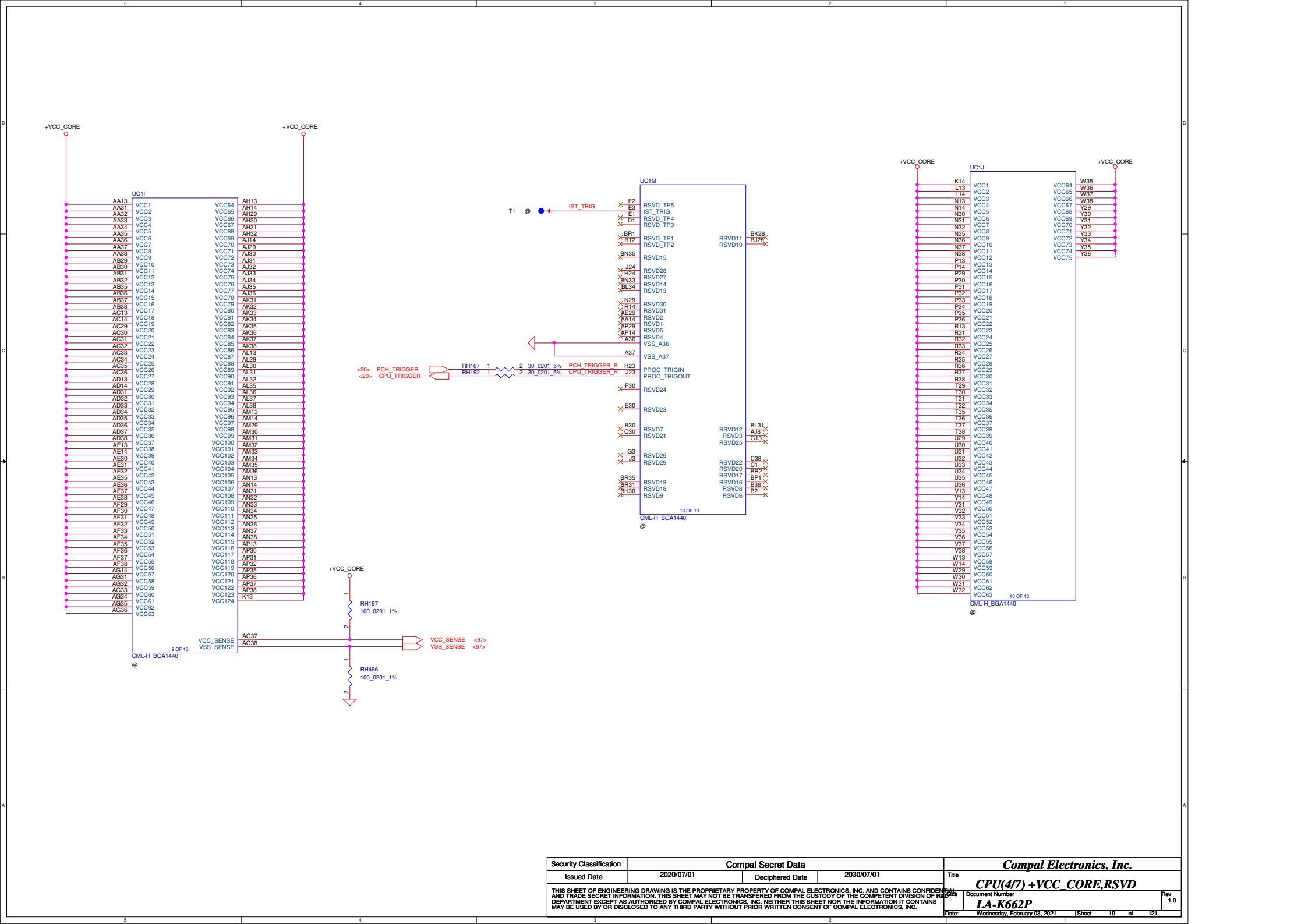


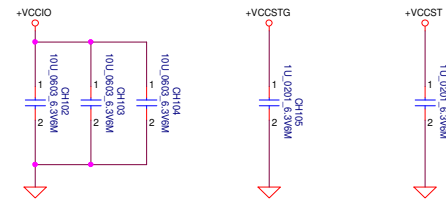
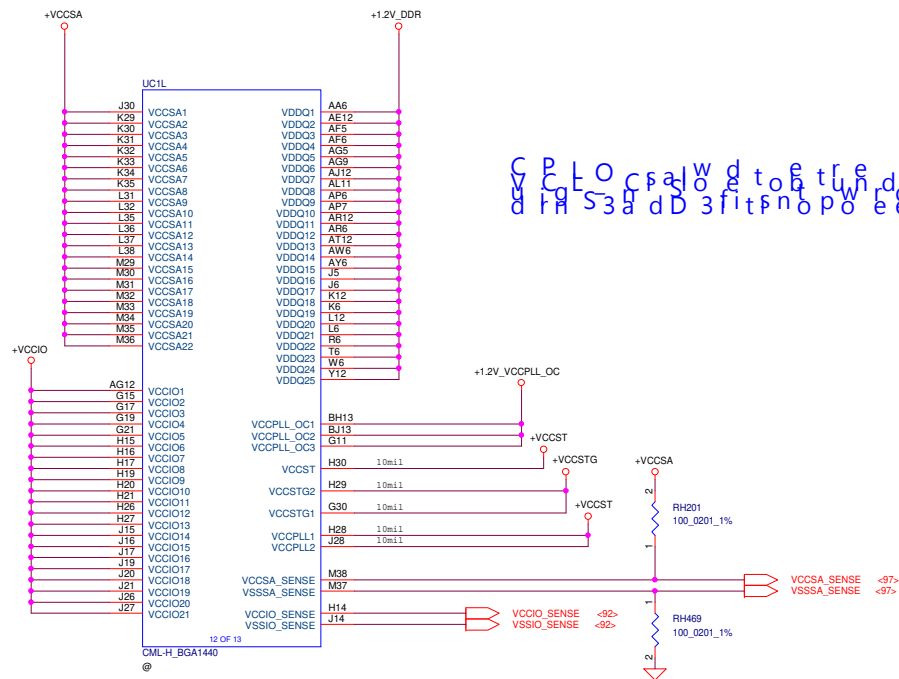
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Net : DDR\_RCOMP1  
Net : DDR\_RCOMP2  
Trace Width/Space: 15 mil  
Max Trace Length: 500 mil

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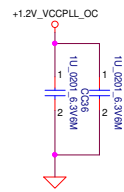
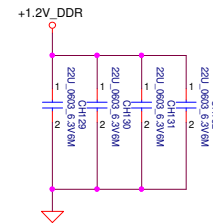
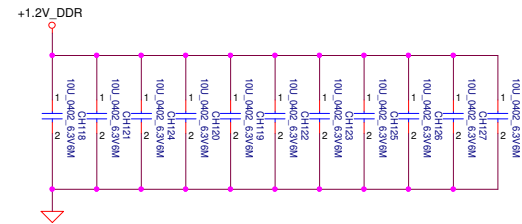




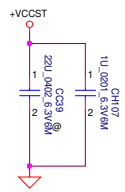
Close to H29,G30

Close to H30

CPLOCSAW d to f t u e d f  
d f H S3 a d B 3 f i t f n o p o e e d r e t y r m v B Q



Close to BH13,BJ13,G11

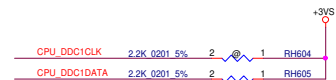
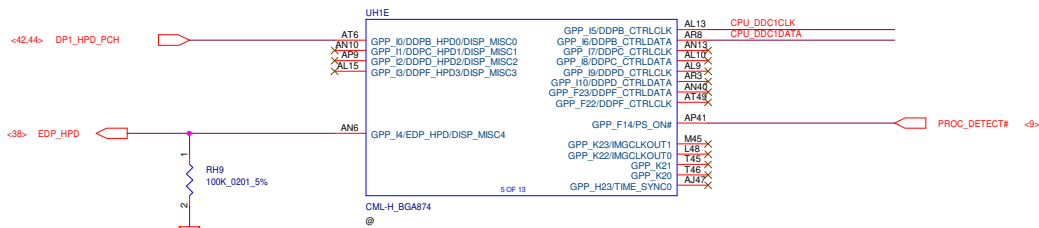
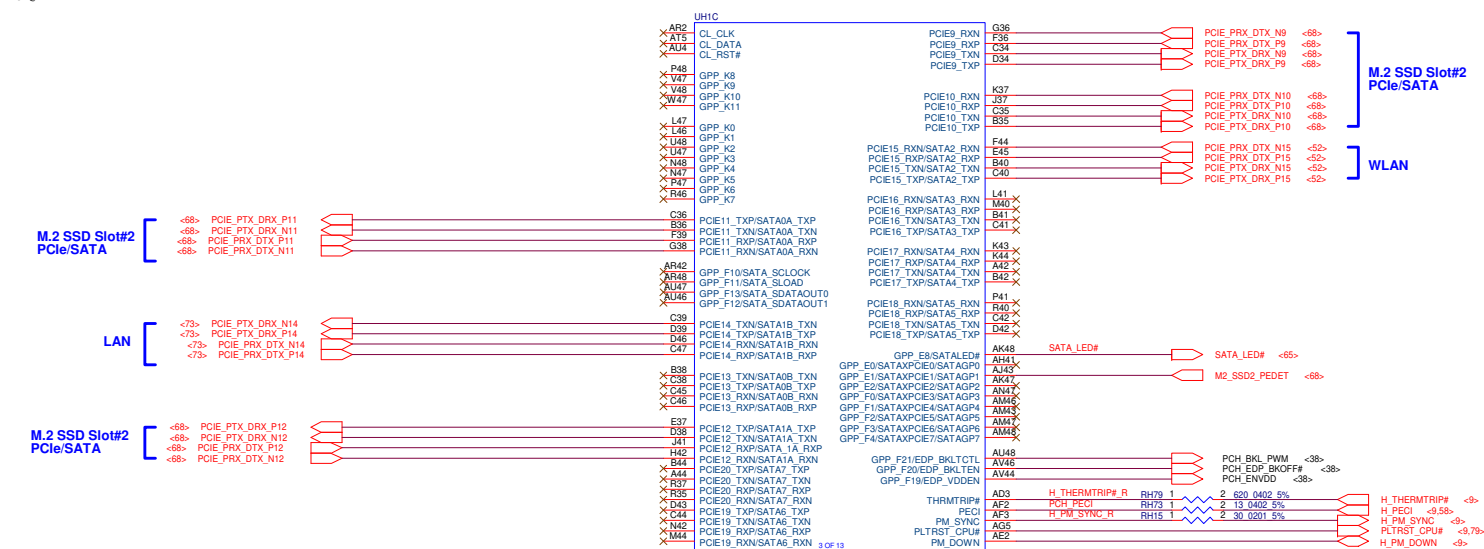


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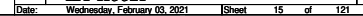
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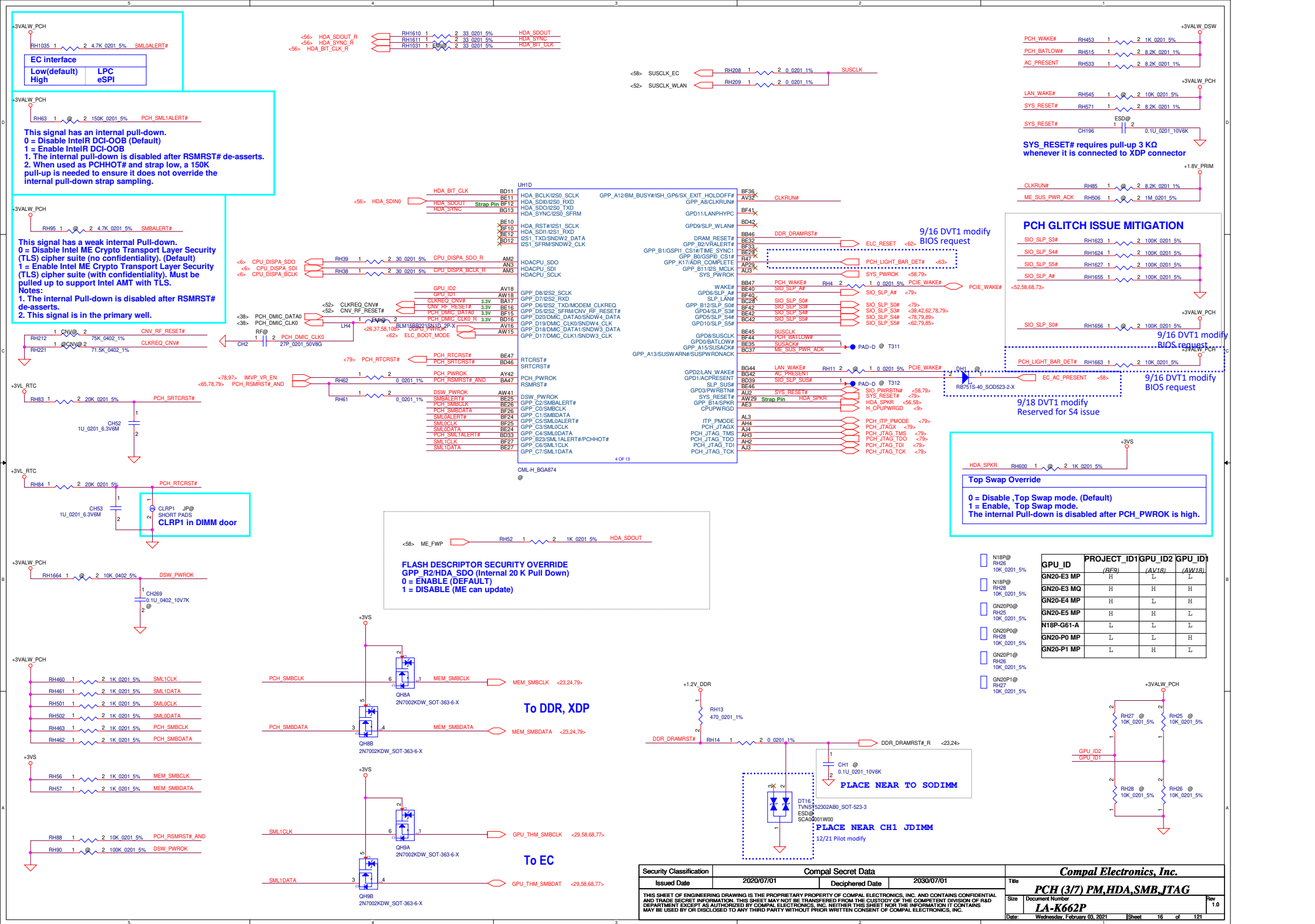




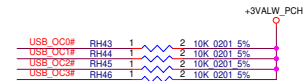
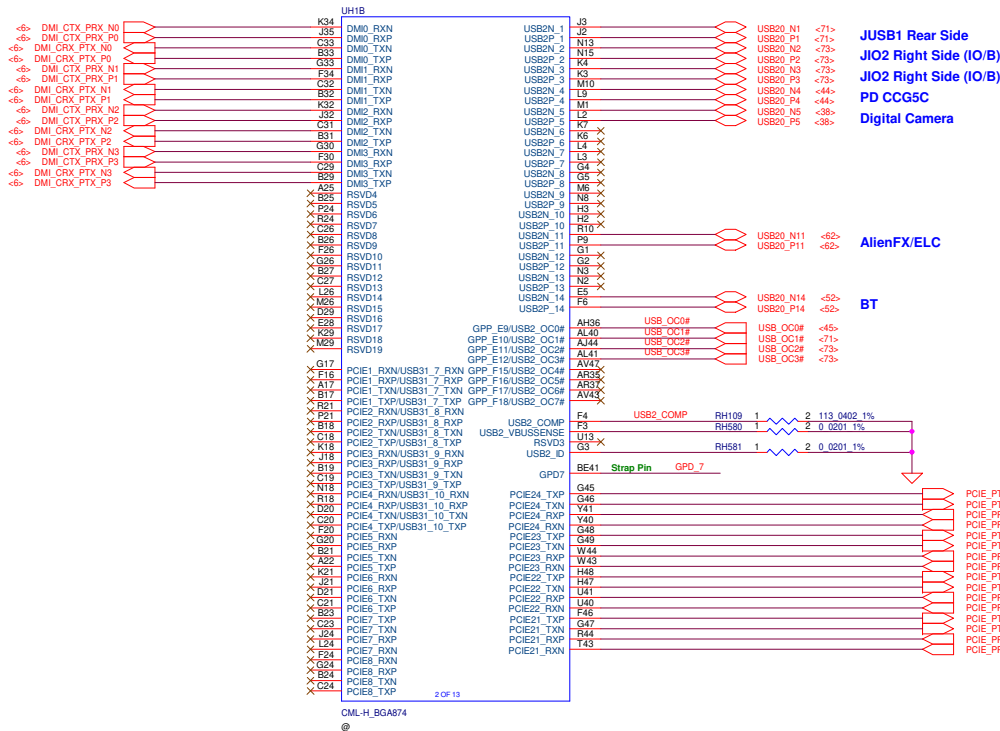


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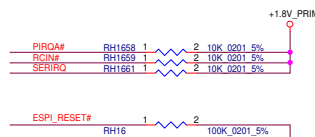
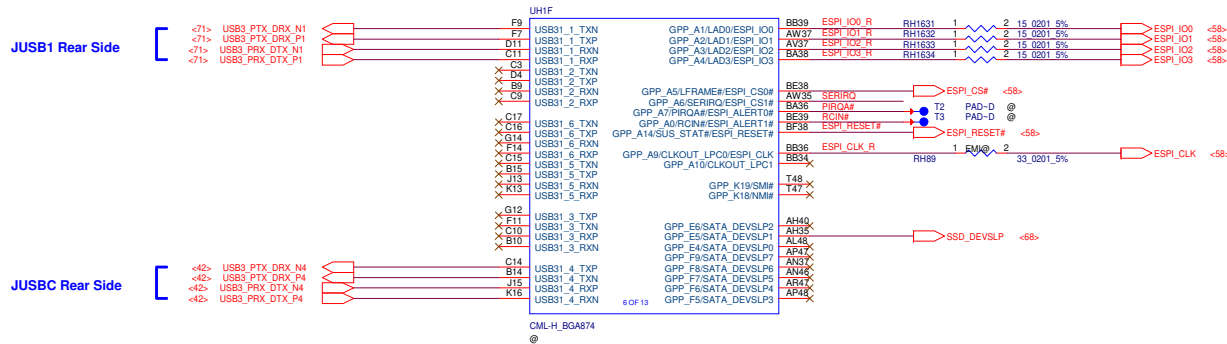
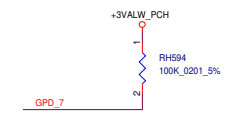


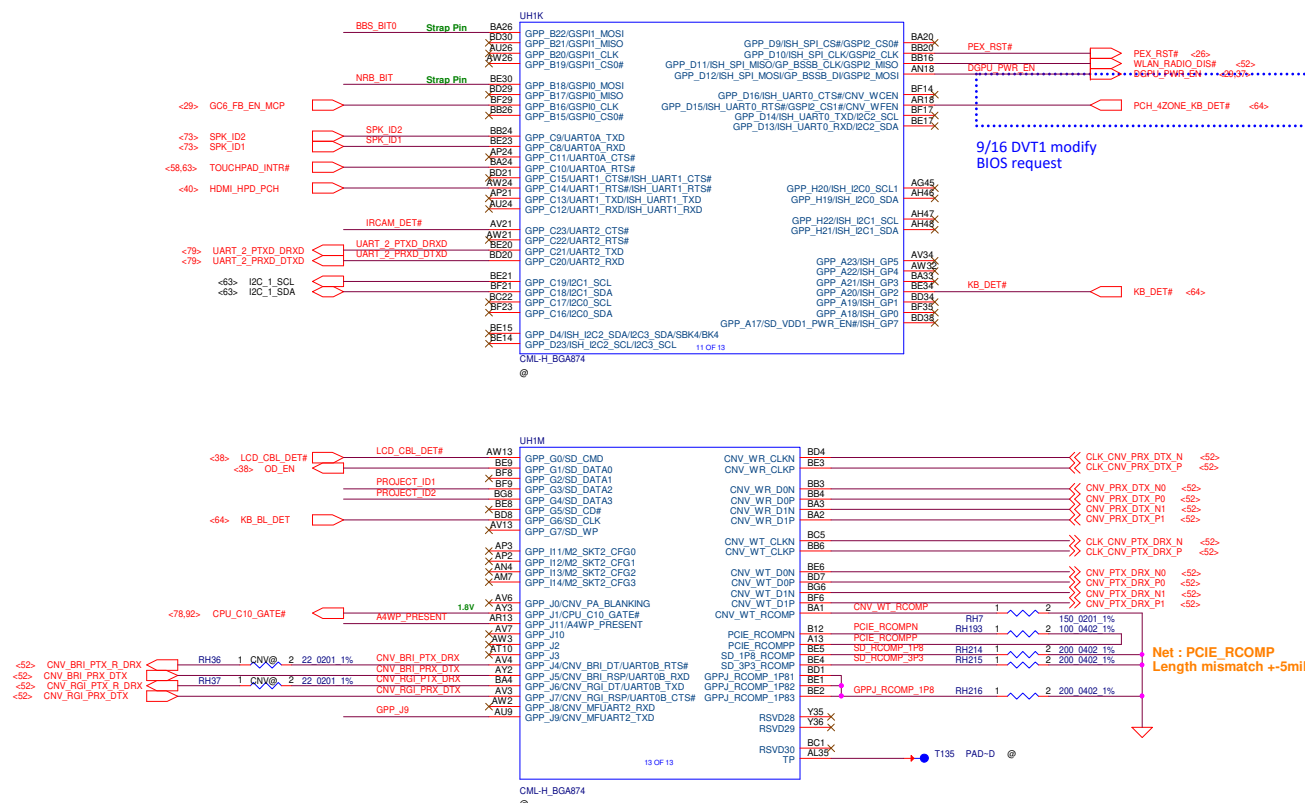
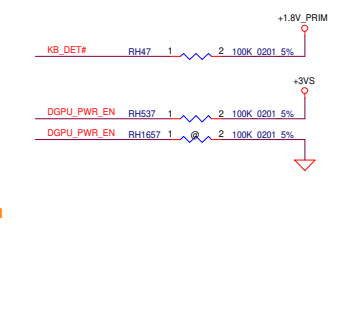
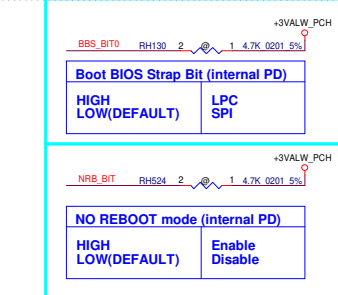
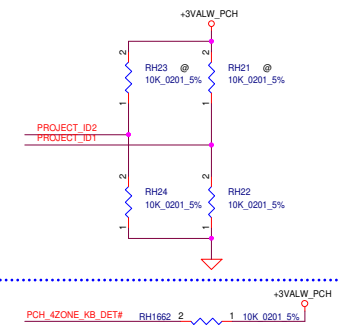






GPIO	Device Control
USB_OC0#	USB Type-C (MB)
USB_OC1#	USB3 Port 1 (MB)
USB_OC2#	USB3 Port 2 (DB)
USB_OC3#	USB3 Port 3 (DB)

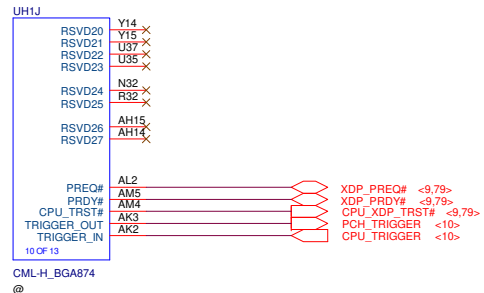
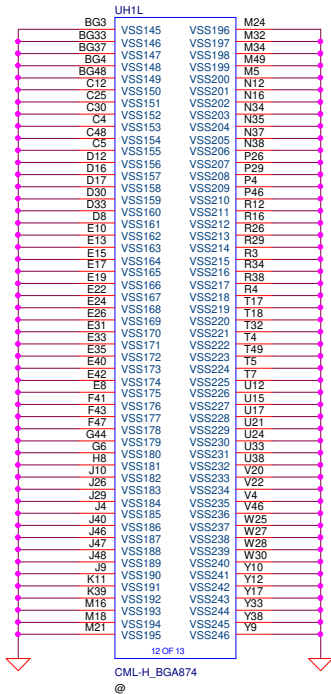
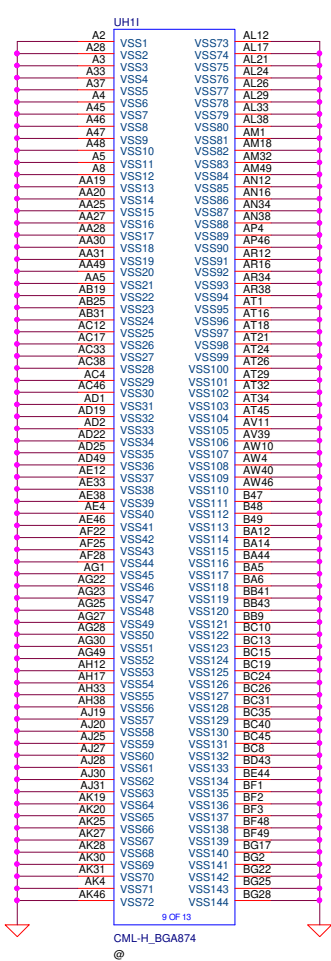




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Main Function:

Reserve

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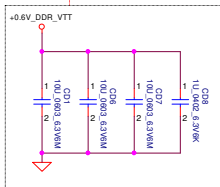
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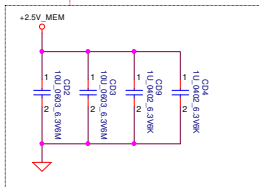
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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 22 of 121

**Main Func = DDR**

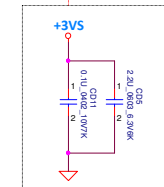
Layout Note:  
Place near JDIMM1 250



Layout Note:  
Place near JDIMM1 257 259



Layout Note:  
Place near JDIMM1 255



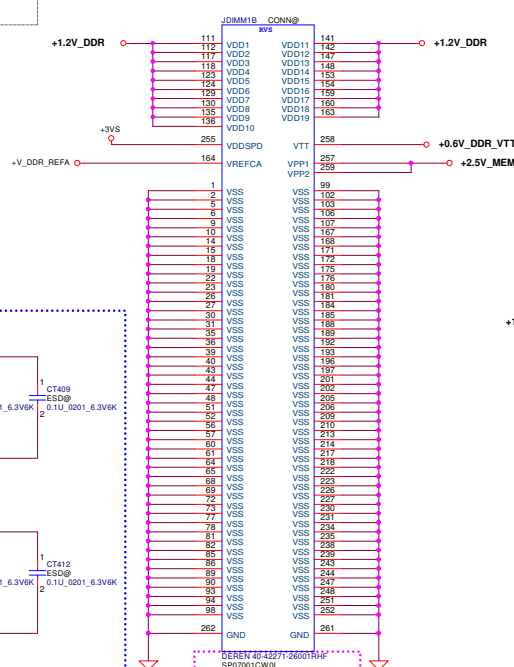
## Interleaved Memory

<8> DDR\_M0\_D[0..15]  

<8> DDR\_M0\_D[16..31]  

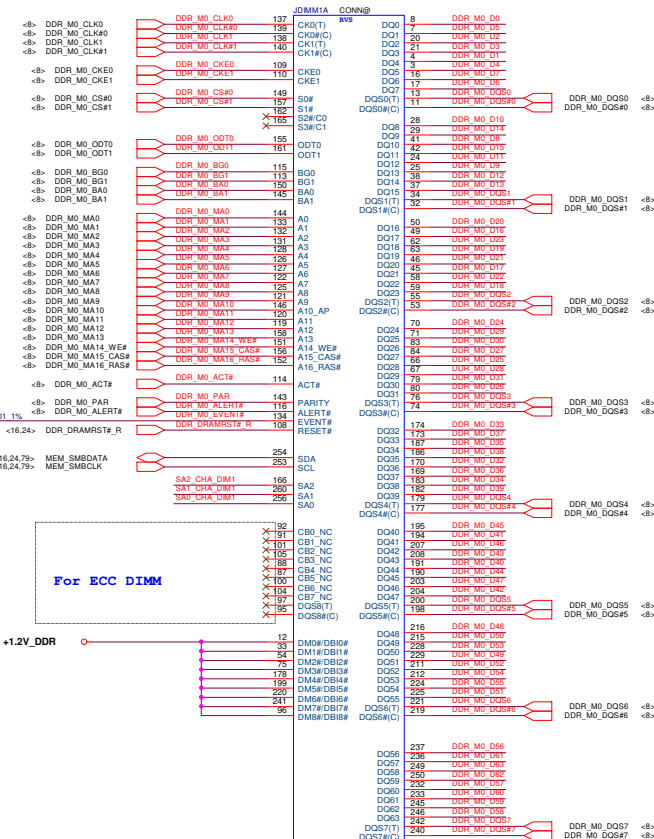
<8> DDR\_M0\_D[32..47]  

<8> DDR\_M0\_D[48..63]  

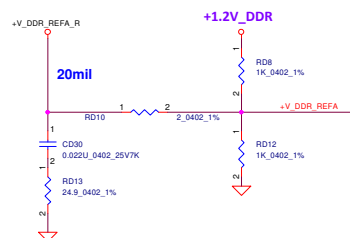
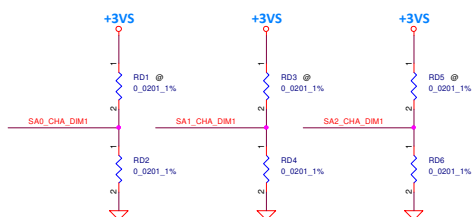


Part Number: SP07001CW0L  
Part Value: S SOCKET DEREN 40-42271-26001RHF DDR A31

**REVERSE TYPE (4 mm)**



DEREN 40-42271-26  
SP07001CW01

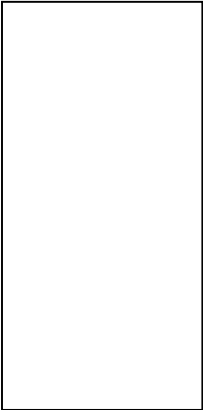


























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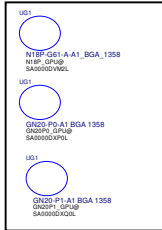


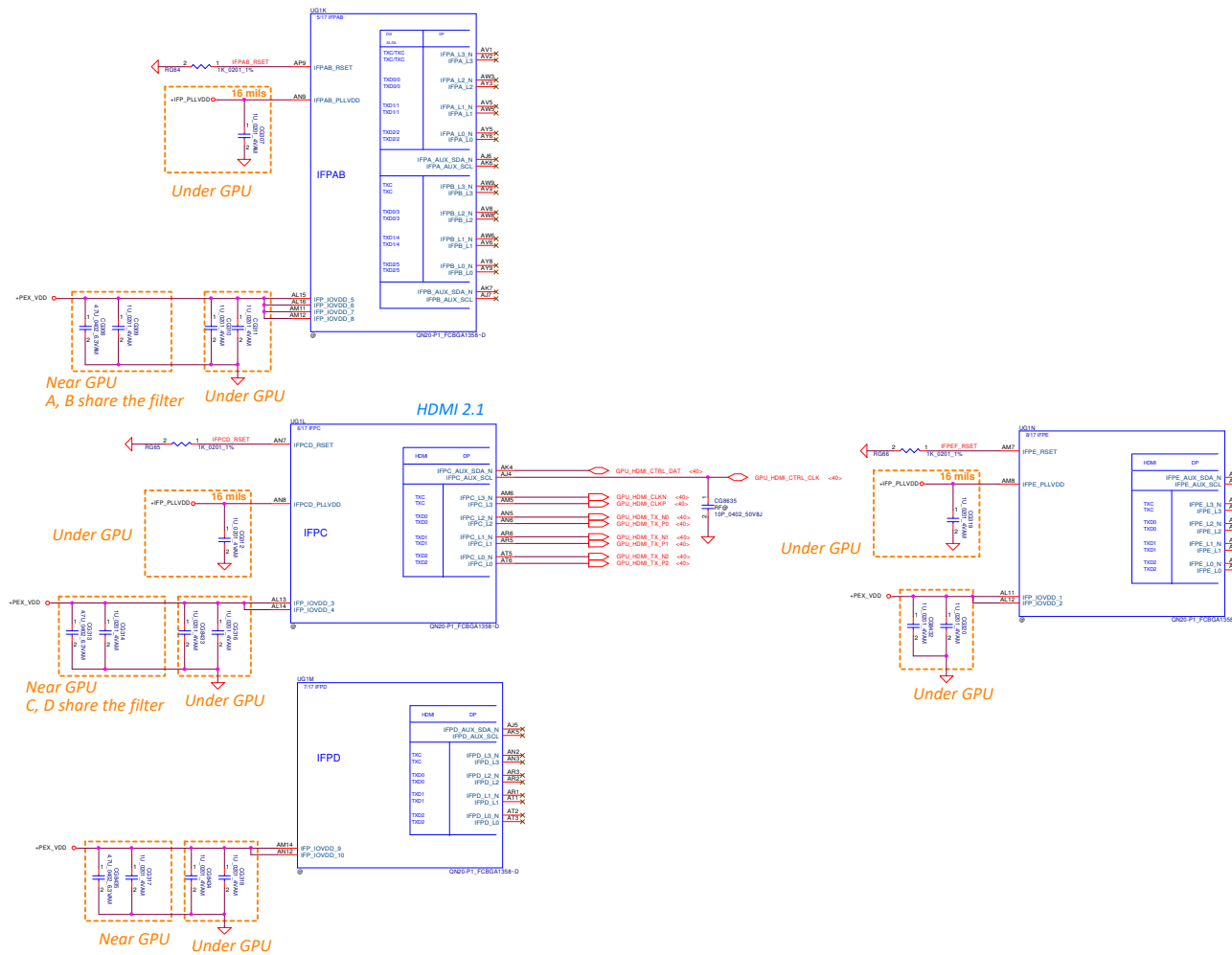


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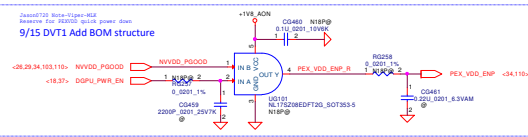
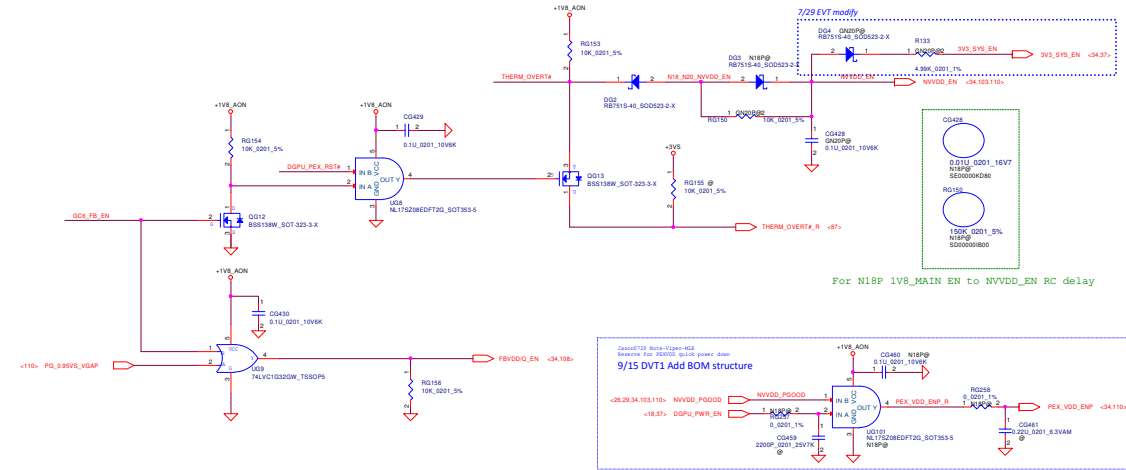
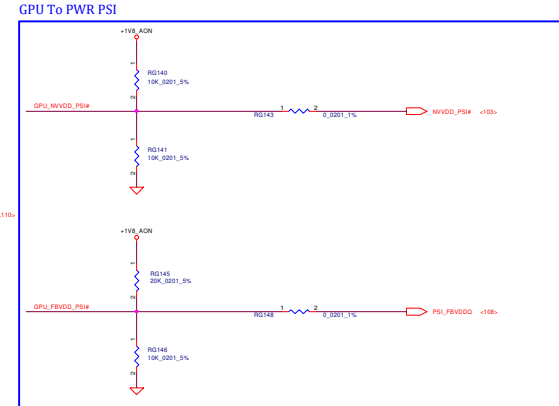
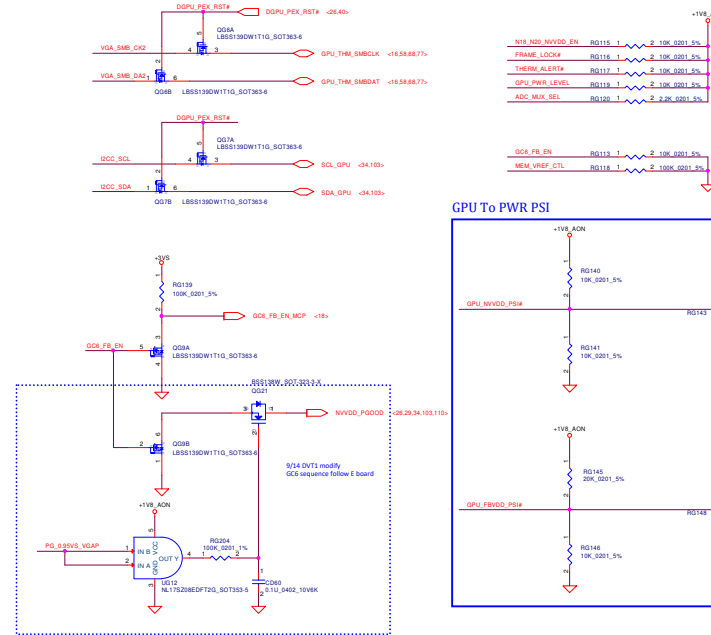
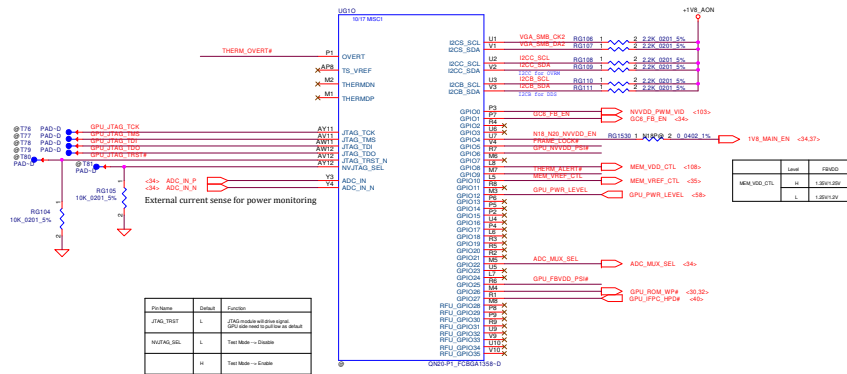


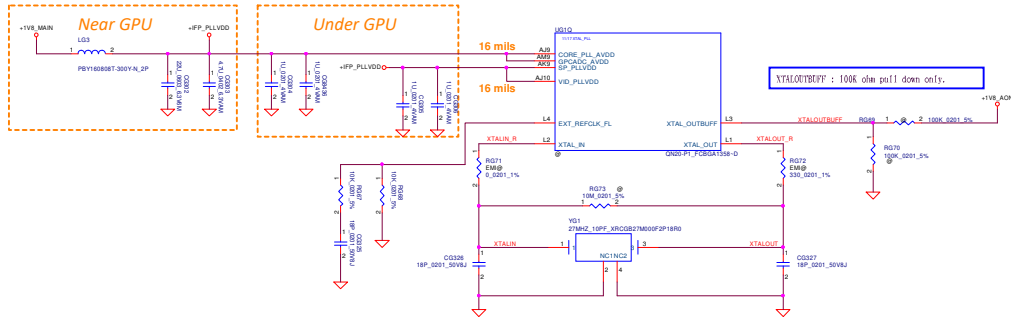
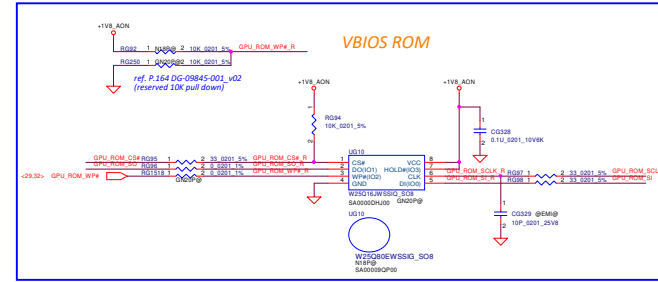
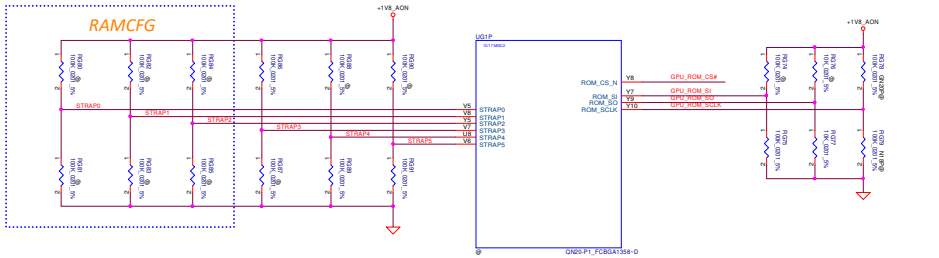
8G bit GDDR6					
Micron 4GB SKU		Samsung 4GB SKU		Hynix 4GB SKU	
R1	R3	R1	R3	R1	R3
<div>UM6 VMBGR3@  MT61K256M3ZJE-14-A1.2V SA000BND7L  100K + 5% 0201 SD043100380</div> <div>UM10 VMBGR3@  MT61K256M3ZJE-14-A1.2V SA000BND7L  100K + 5% 0201 SD043100380</div> <div>UM11 VMBGR3@  MT61K256M3ZJE-14-A1.2V SA000BND7L  100K + 5% 0201 SD043100380</div> <div>UM12 VMBGR3@  MT61K256M3ZJE-14-A1.2V SA000BND7L</div>	<div>RG01 VMB@  100K + 5% 0201 SD043100380</div> <div>RG02 VMB@  100K + 5% 0201 SD043100380</div> <div>RG03 VMB@  100K + 5% 0201 SD043100380</div> <div>RG04 VMB@  100K + 5% 0201 SD043100380</div>	<div>UM6 VMBGR3@  K4Z8D3258BC-HC14 1.2V SA0000C6EL  100K + 5% 0201 SD043100380</div> <div>UM10 VMBGR3@  K4Z8D3258BC-HC14 1.2V SA0000C6EL  100K + 5% 0201 SD043100380</div> <div>UM11 VMBGR3@  K4Z8D3258BC-HC14 1.2V SA0000C6EL  100K + 5% 0201 SD043100380</div> <div>UM12 VMBGR3@  K4Z8D3258BC-HC14 1.2V SA0000C6EL</div>	<div>RG01 VSB@  100K + 5% 0201 SD043100380</div> <div>RG02 VSB@  100K + 5% 0201 SD043100380</div> <div>RG03 VSB@  100K + 5% 0201 SD043100380</div> <div>RG04 VSB@  100K + 5% 0201 SD043100380</div>	<div>UM6 VMBGR1@  H56C2H24AAR-S2C SA0000DUWL  100K + 5% 0201 SD043100380</div> <div>UM10 VMBGR1@  H56C2H24AAR-S2C SA0000DUWL  100K + 5% 0201 SD043100380</div> <div>UM11 VMBGR1@  H56C2H24AAR-S2C SA0000DUWL  100K + 5% 0201 SD043100380</div> <div>UM12 VMBGR1@  H56C2H24AAR-S2C SA0000DUWL</div>	<div>RG01 VMB@  100K + 5% 0201 SD043100380</div> <div>RG02 VMB@  100K + 5% 0201 SD043100380</div> <div>RG03 VMB@  100K + 5% 0201 SD043100380</div> <div>RG04 VMB@  100K + 5% 0201 SD043100380</div>

[illegible]





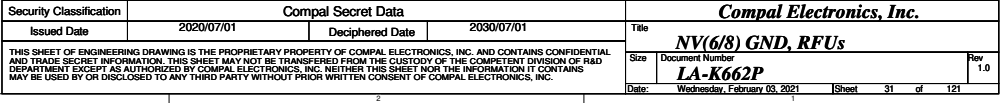


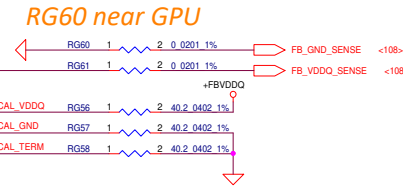
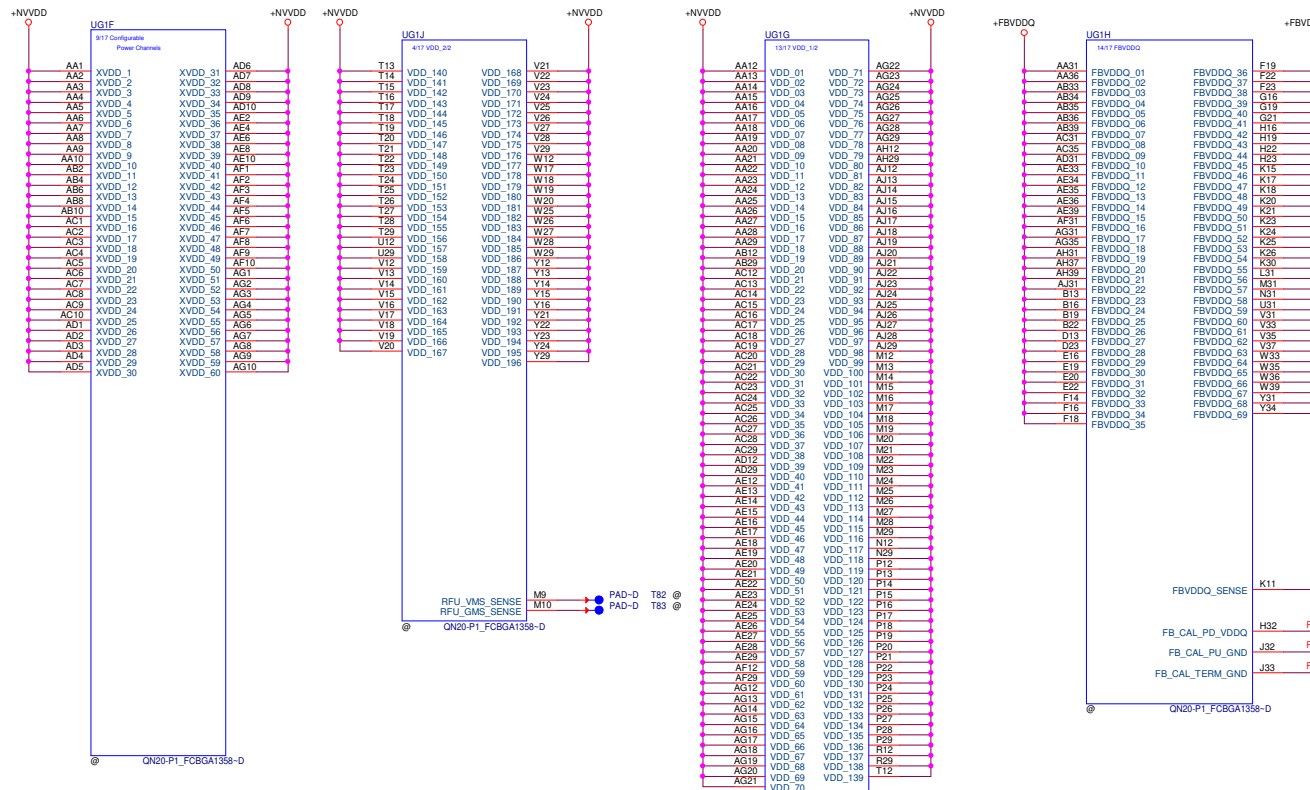


STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
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M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

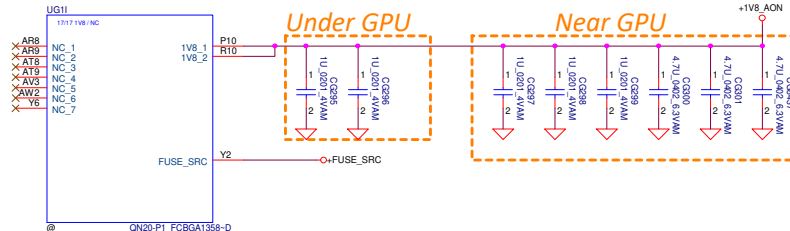
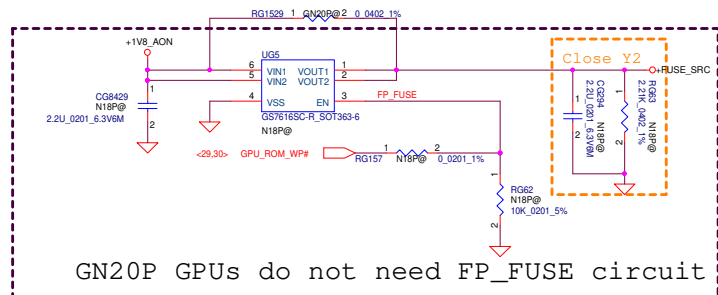
- 1:SMB\_ALT\_ADDR ENABLE
- 0:SMB\_ALT\_ADDR DISABLE
- 1:DEVID\_SEL REBRAND
- 0:DEVID\_SEL ORIGINAL
- 1:PCIE\_CFG LOW POWER
- 0:PCIE\_CFG HIGH POWER
- 1:VGA\_DEVICE ENABLE
- 0:VGA\_DEVICE DISABLE

Default





# FUSE\_SRC

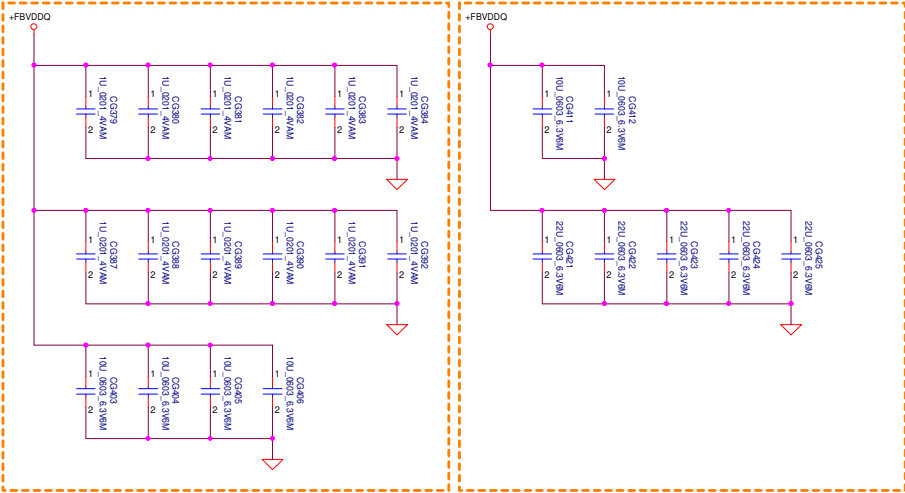




FBVDDQ\_GPU

Under GPU

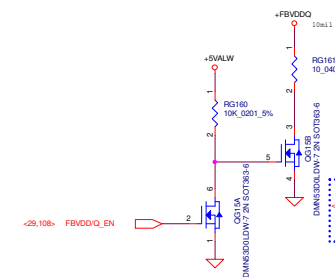
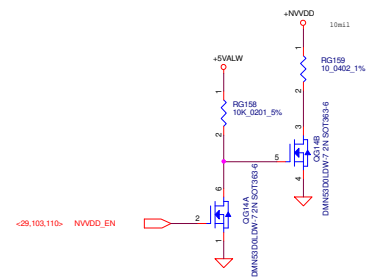
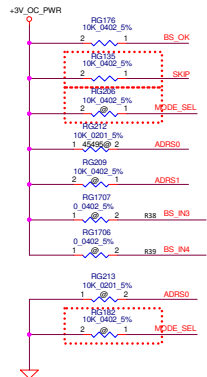
Near GPU



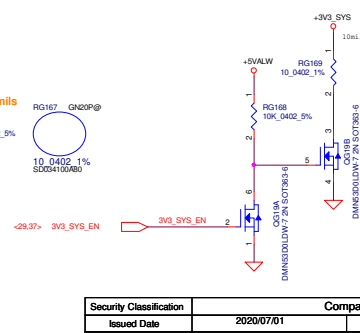
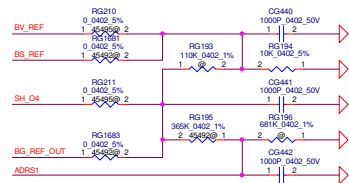
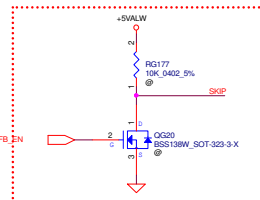
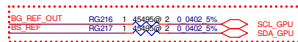
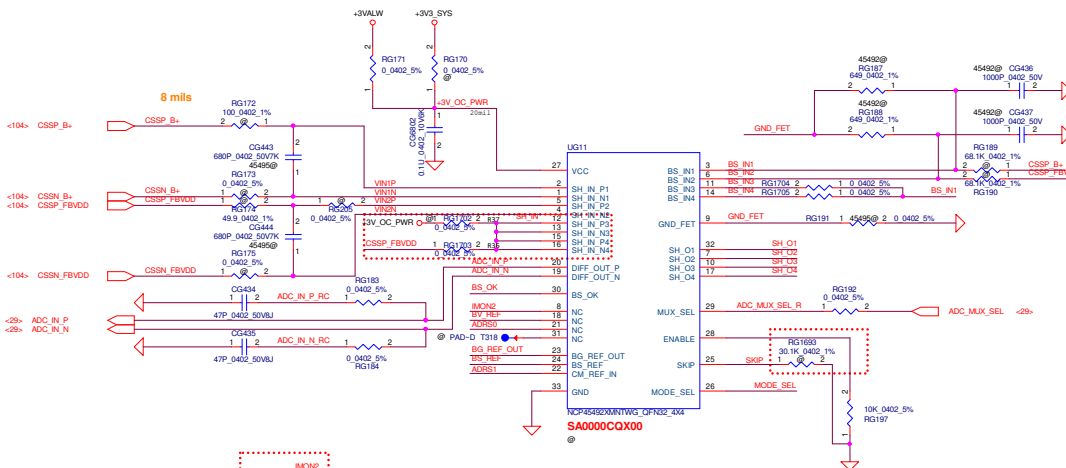
UG11

## OVRM Gen2 with GN20P0/P1

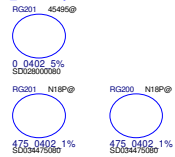
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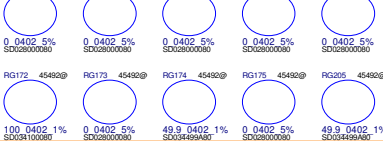
9/15 DVT1 modify  
For GPU sequence



RG201 45495@



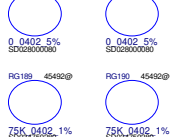
RG172 45495@



RG196 45495@



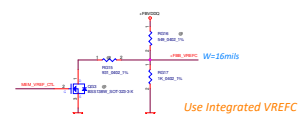
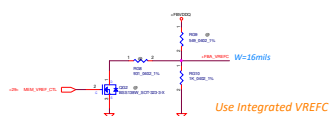
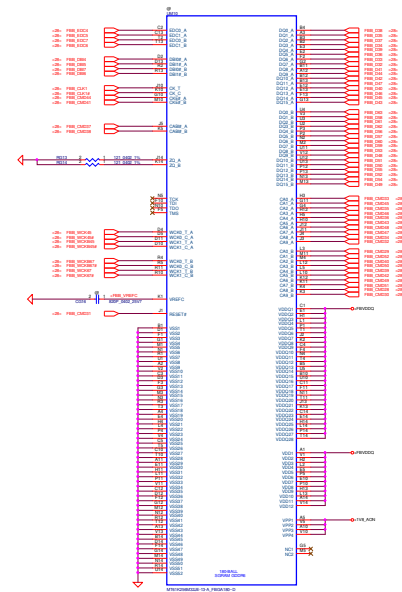
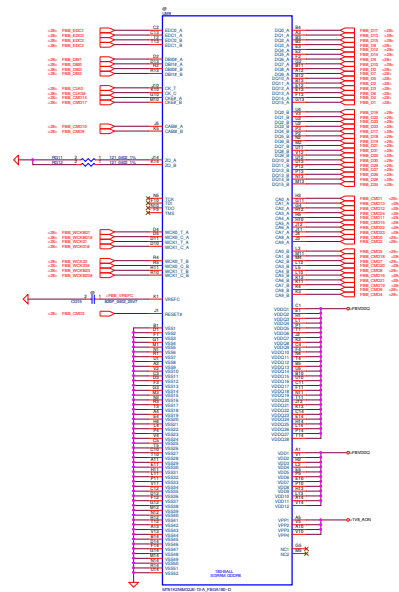
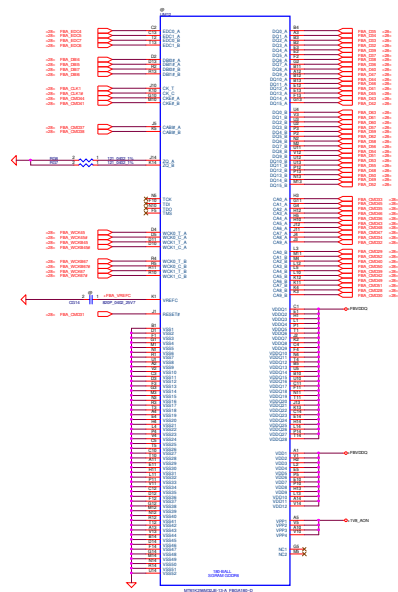
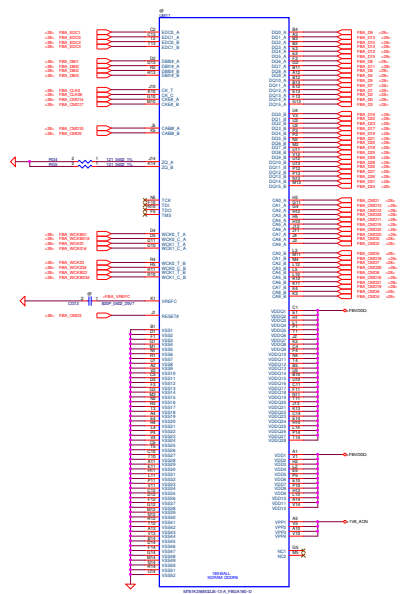
RG189 45495@



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Date: 2020.07.01 09:00:01 Decoded: 24.07.2025				

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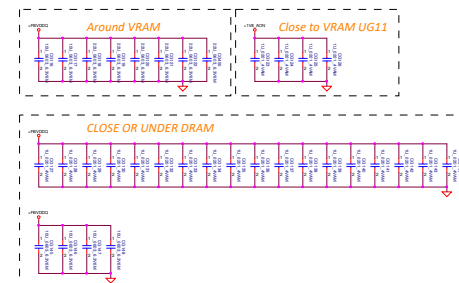
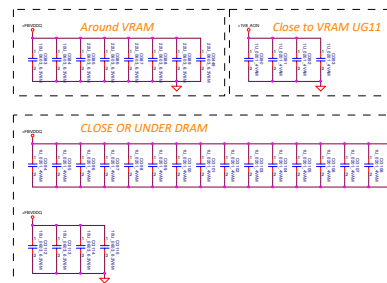
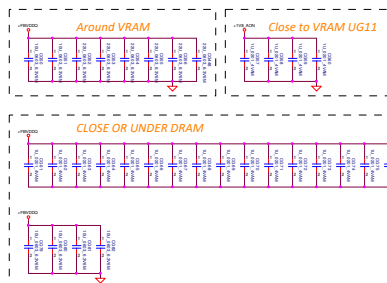
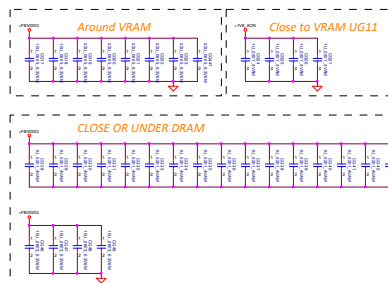


*UM11*

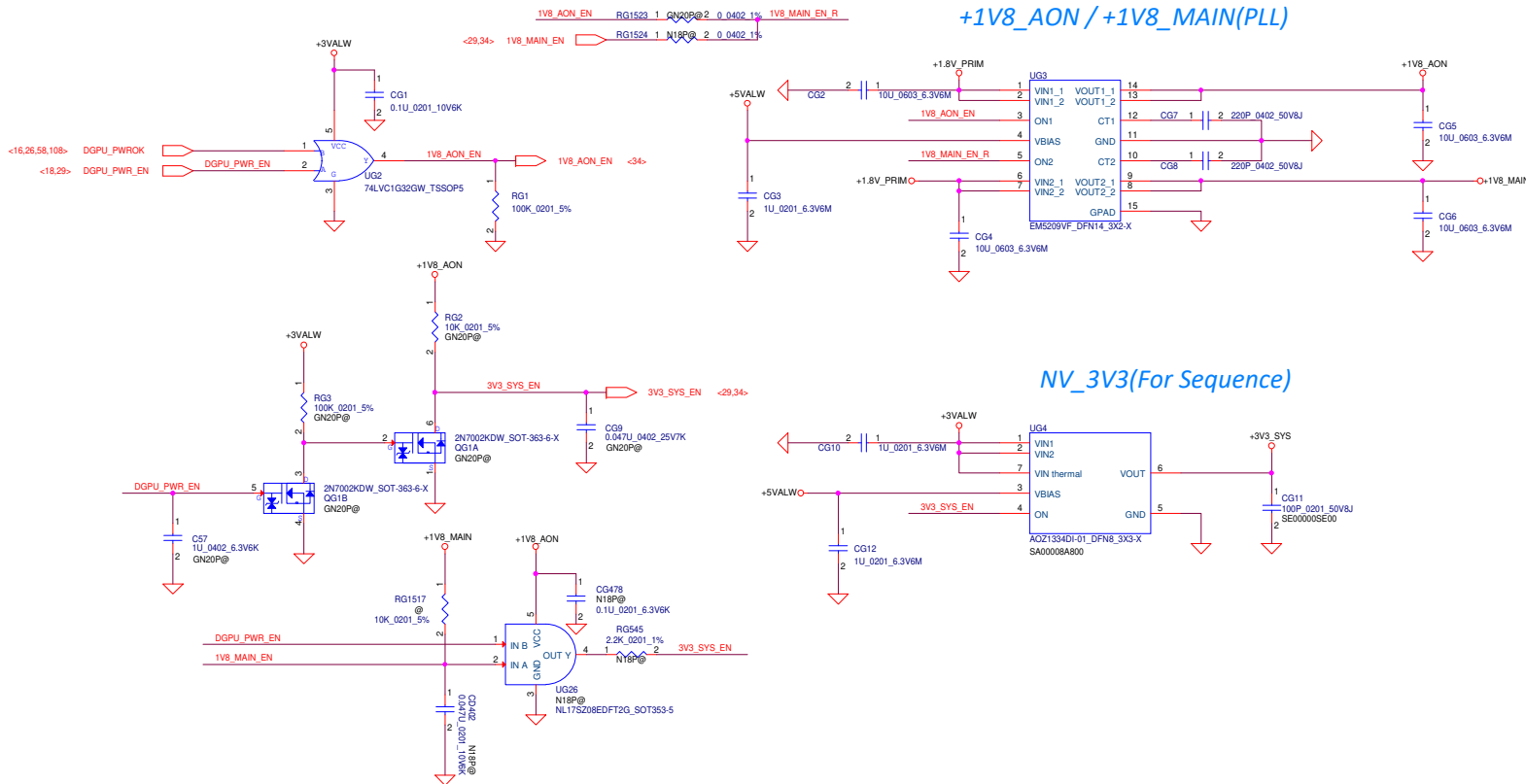
UM12

UM9

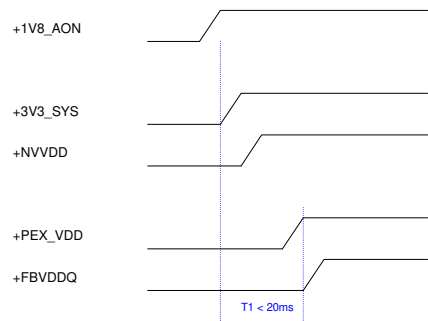
UM10





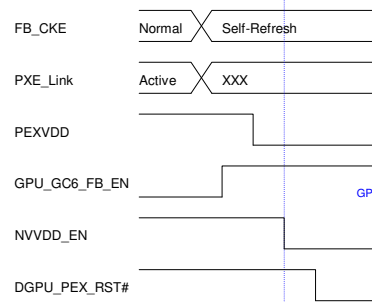


## GPU Power Up Sequence



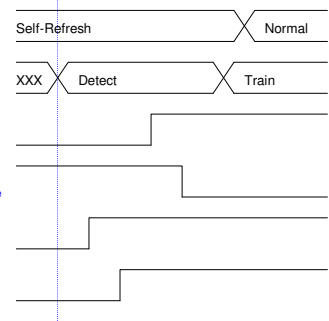
The ramp time for any rail must be more than 40us and less than 2ms.

## GPU GC6 Entry Sequence

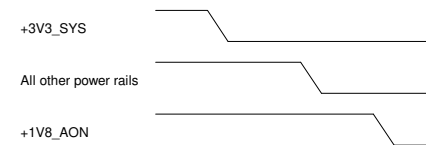


The entire entry/exit sequence must complete within 200 ms.

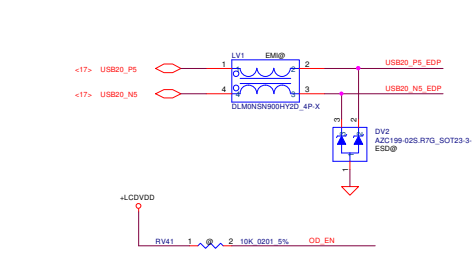
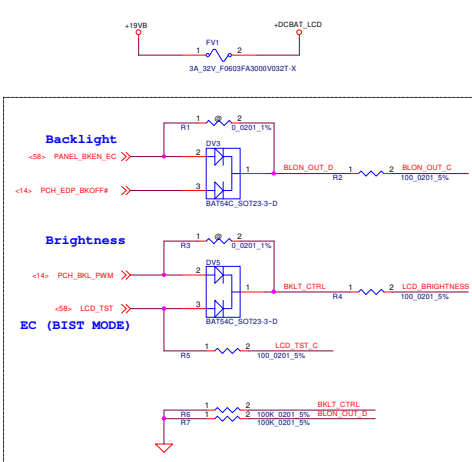
## GPU GC6 Exit Sequence



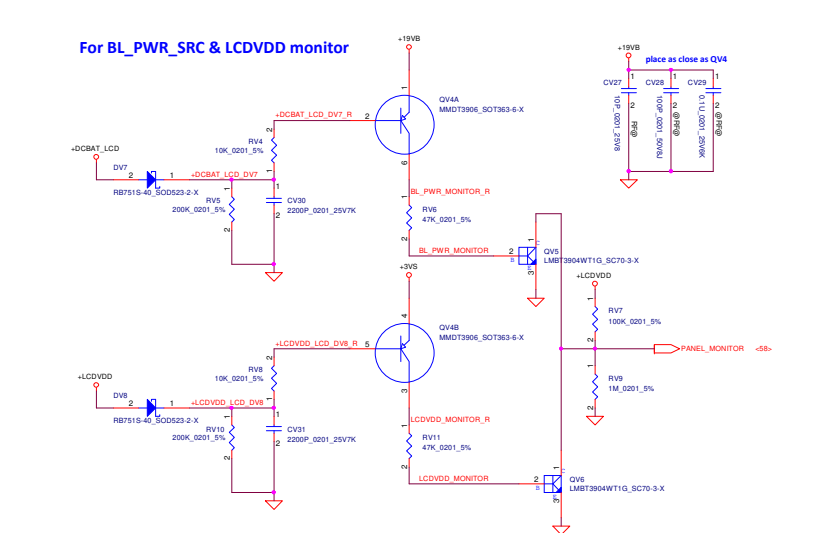
## GPU Power Down Sequence



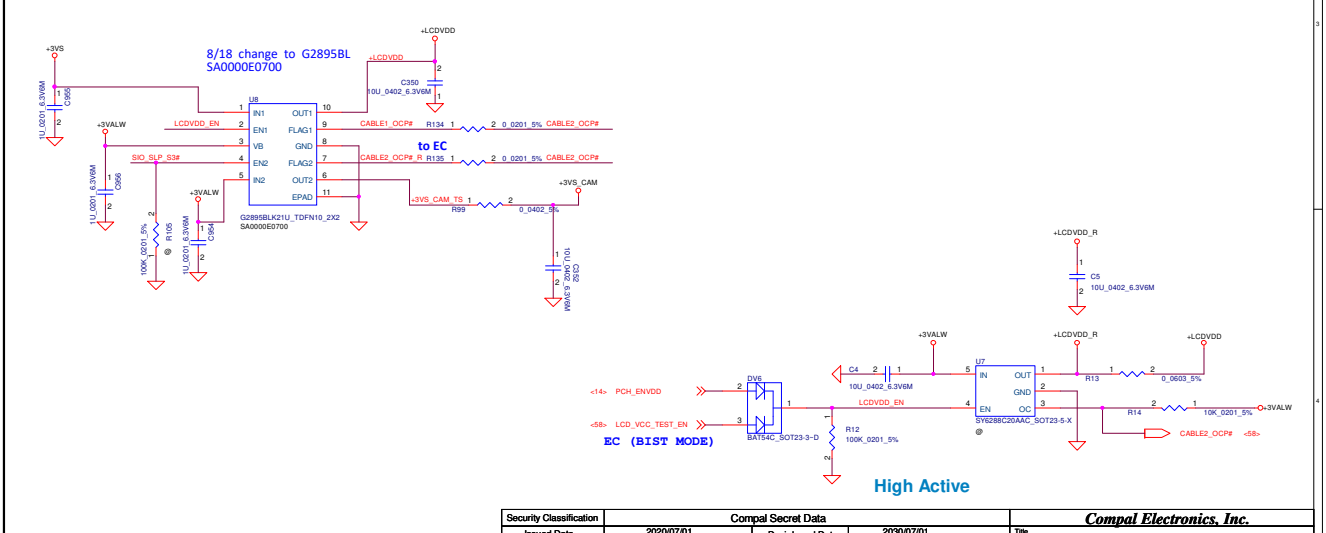
Main Func = LCD



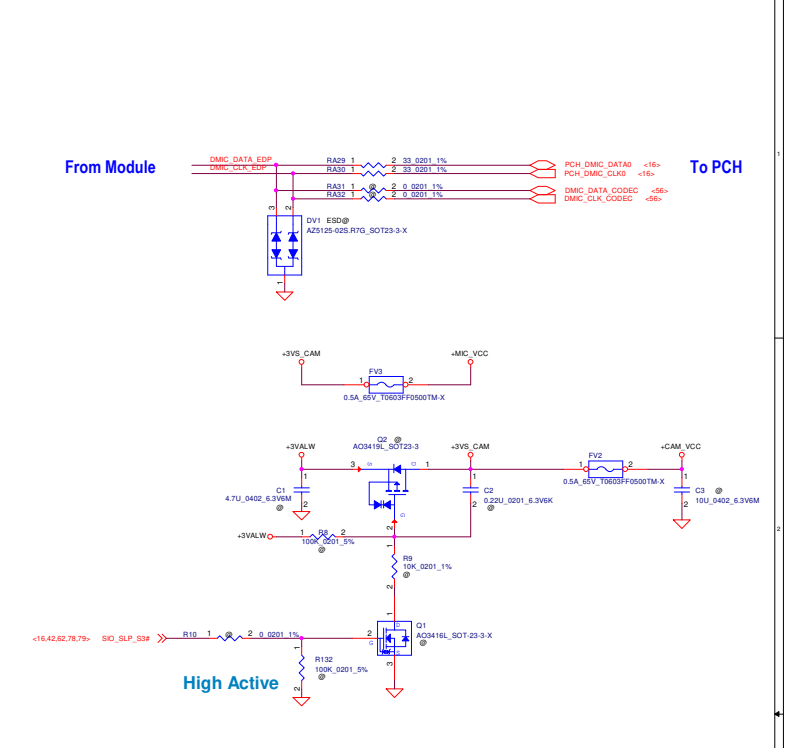
Main Func = LCDVDD monitor



Main Func = Hinge up protection



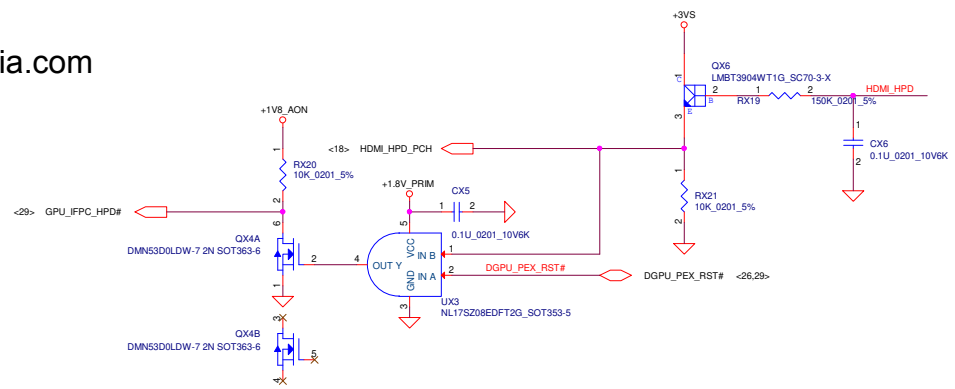
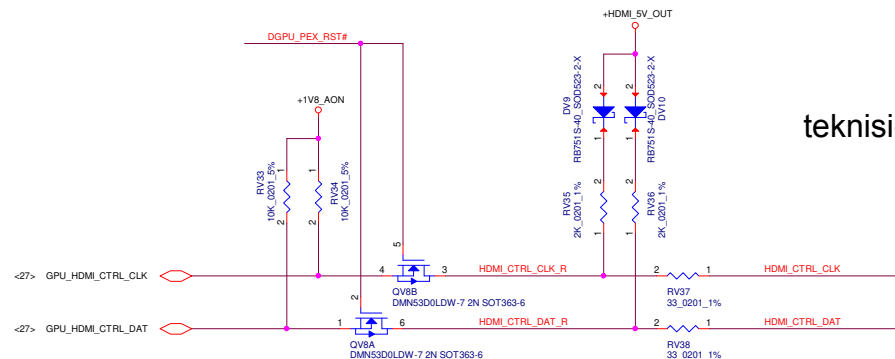
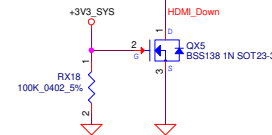
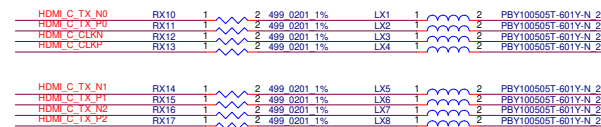
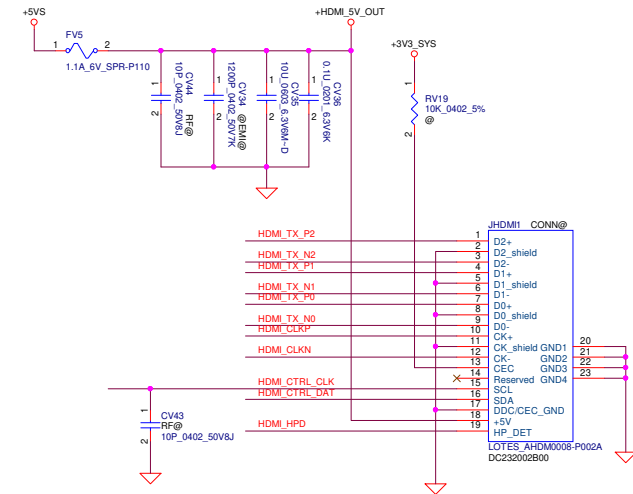
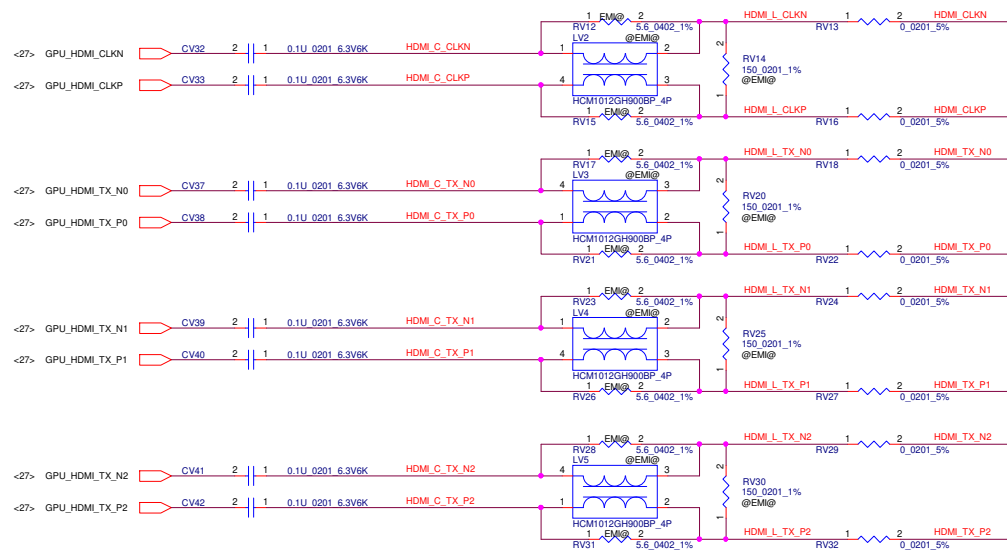
Main Func = DMIC



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Main Func = DDS

Main Func = eDP MUX



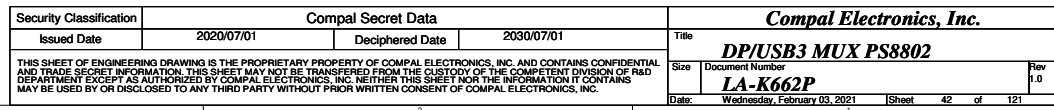
teknisi-indonesia.com



Main Function:

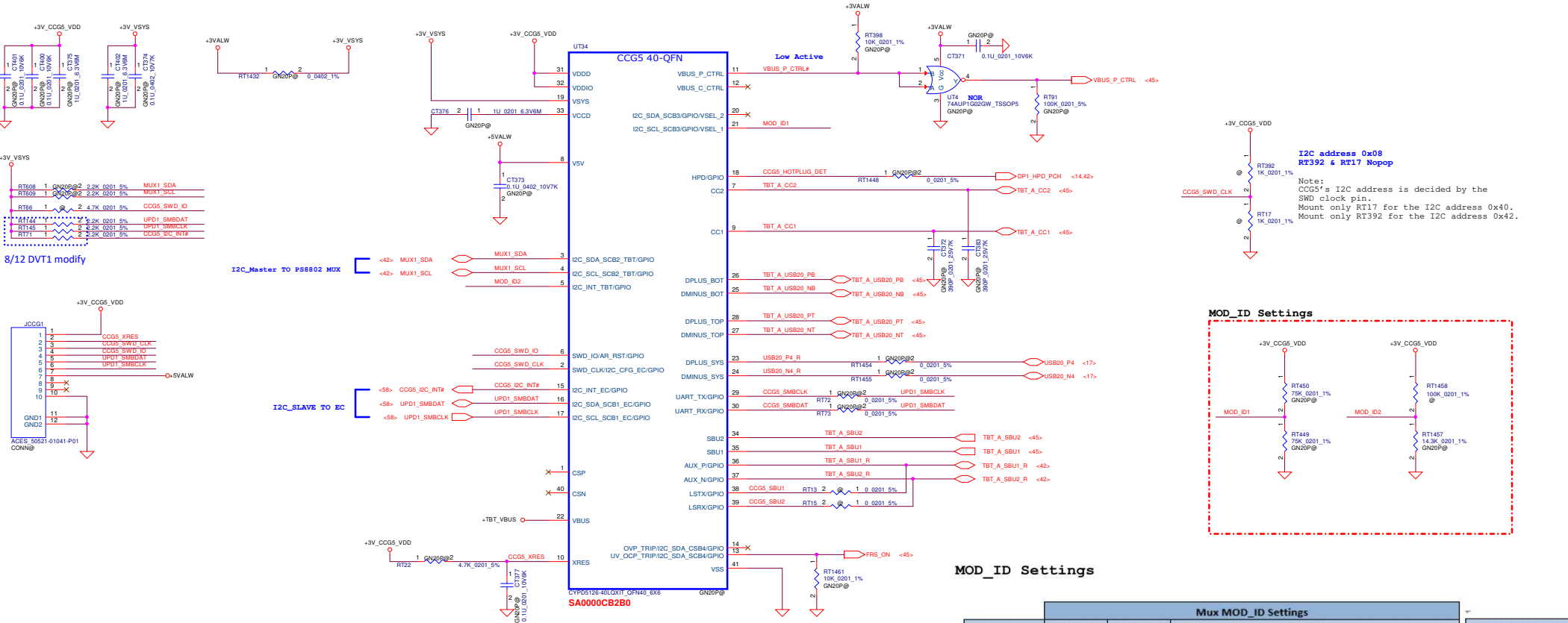
Reserve

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				Date:	Wednesday, February 03, 2021	Sheet 41 of 121



5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

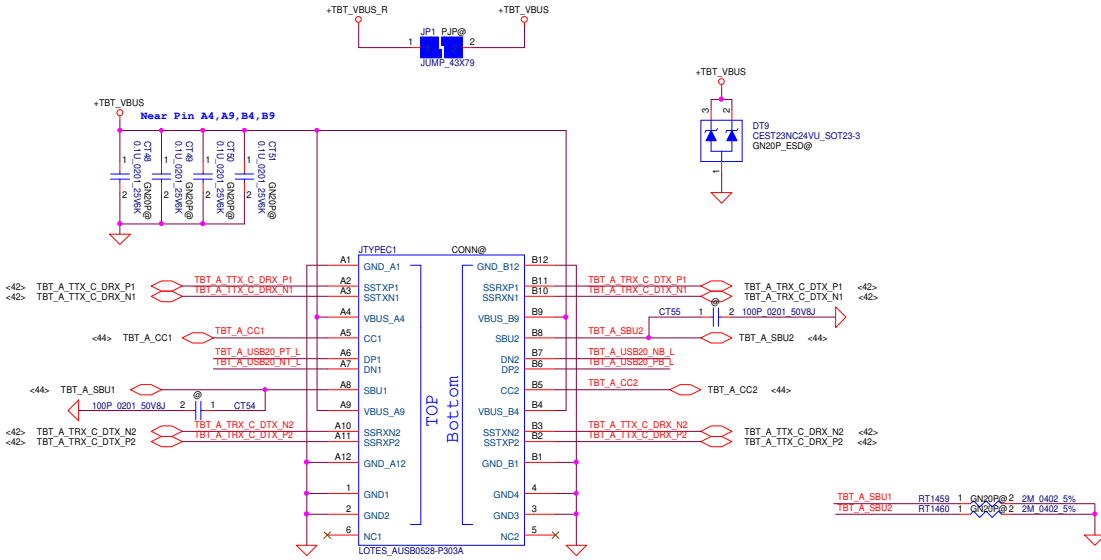
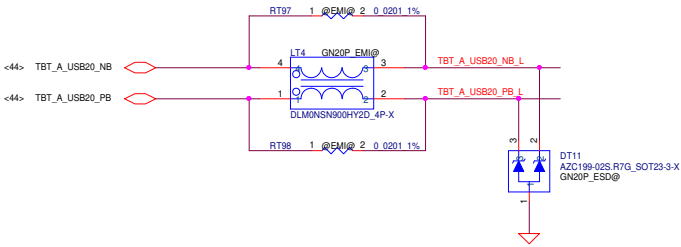
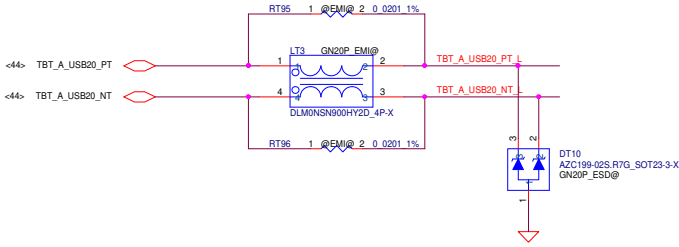
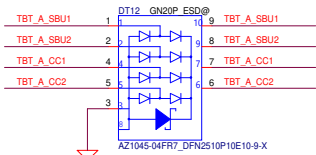
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2020/07/01	Deciphered Date	2030/07/01	Title	Thunderbolt (2/2)
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			Date:	Wednesday, February 03, 2021	Sheet 43 of 121



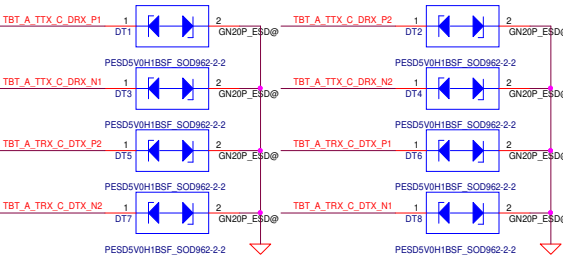
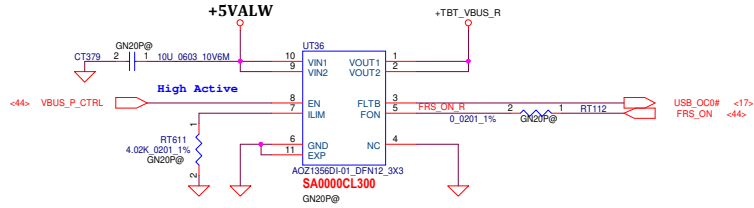
MOD\_ID Settings

Mux MOD_ID Settings				
MUX	MOD_ID1	MOD_ID2	Description	Voltage Levels <sup>1</sup>
Titan Ridge	L1	N/A	TBT Configuration	L0 = 0V <sup>2</sup>
PS8802	L4	L0	PS8802 Equalizer config #1	L1 = VDDD/8 <sup>3</sup>
PS8802	L4	L1 - L3	Reserved for PS8802 Equalizer config #2,3,4 reserved	L2 = 2*VDDD/8 <sup>3</sup>
ANX7443	L5	L0	ANX7443 Equalizer config #1	L3 = 3*VDDD/8 <sup>3</sup>
ANX7443	L5	L1 - L3	Reserved for ANX7443 Equalizer config #2,3,4 reserved	L4 = 4*VDDD/8 <sup>3</sup>
TUSB546	L6	L0	TUSB546 Equalizer config #1	L5 = 5*VDDD/8 <sup>3</sup>
TUSB546	L6	L1 - L3	Reserved for TUSB546 Equalizer config #2,3,4 reserved	L6 = 6*VDDD/8 <sup>3</sup>
TUSB544	L6	L4	TUSB544 Equalizer config #1	L7 = 7*VDDD/8 <sup>3</sup>
TUSB544	L6	L5 - L7	Reserved for TUSB544 Equalizer config #2,3,4 reserved	

Main Function:



Type-C 5V Provide Path Control  
Support PD3.0  
5V@3A



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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 47 of 121

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				Date:	Wednesday, February 03, 2021	Sheet 48 of 121



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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 49 of 121

Main Function:

Reserve

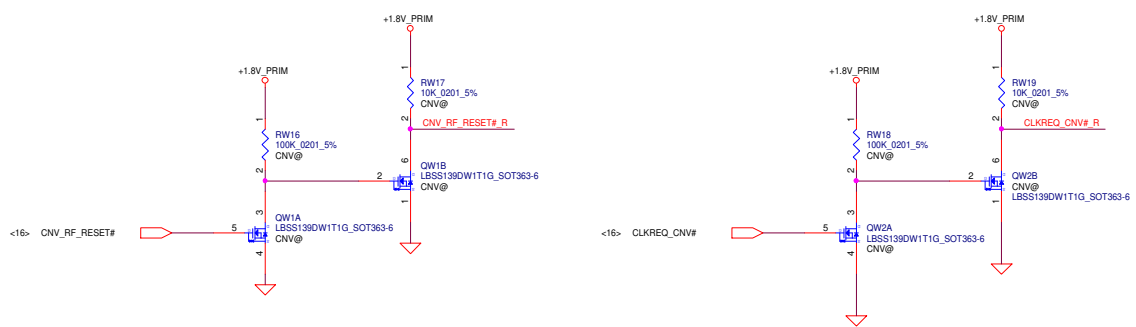
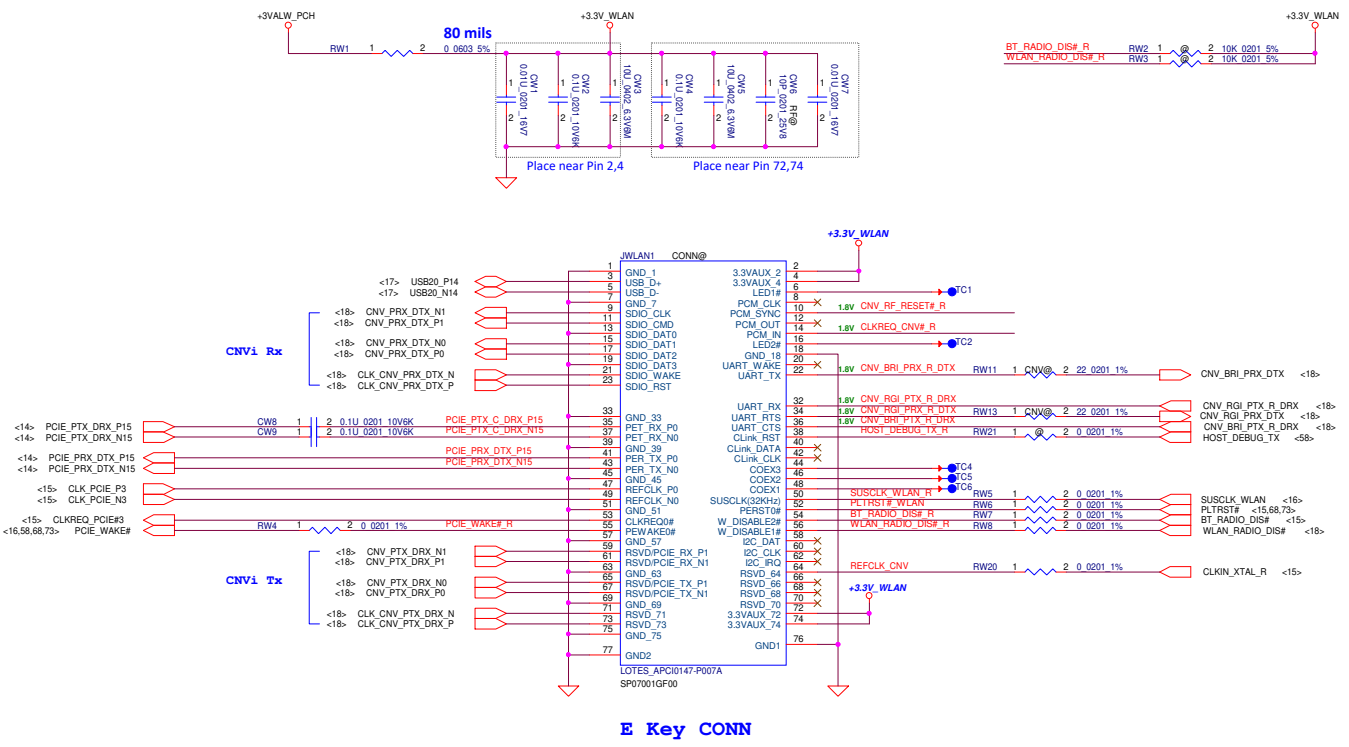
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2020/07/01	Deciphered Date	2030/07/01	Title	RSV	
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				Date:	Wednesday, February 03, 2021	Sheet 50 of 121

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Main Func = WLAN M.2



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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 53 of 121

Main Function:

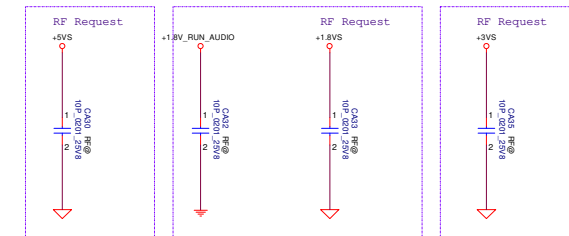
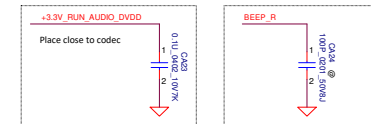
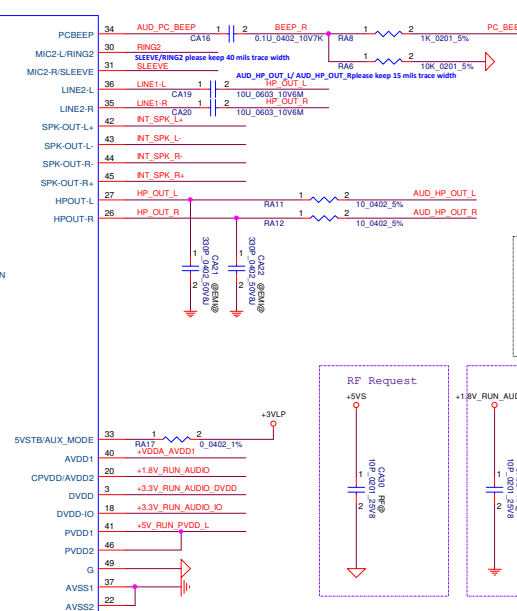
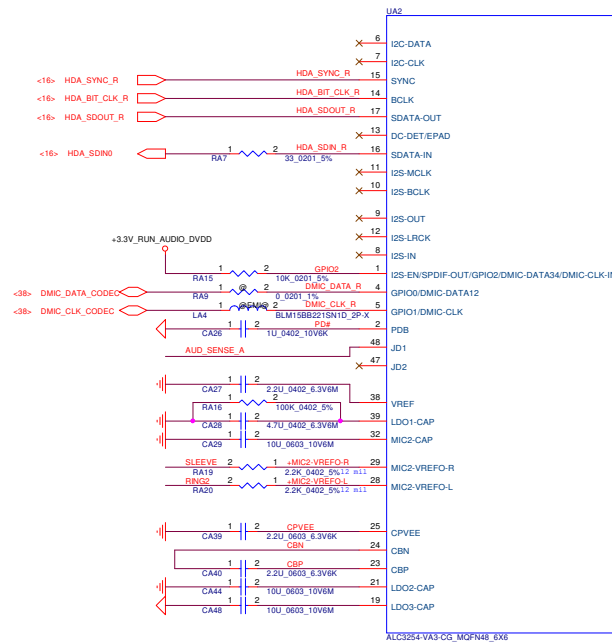
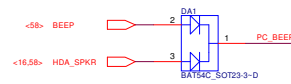
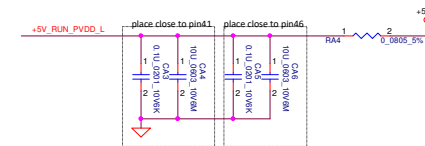
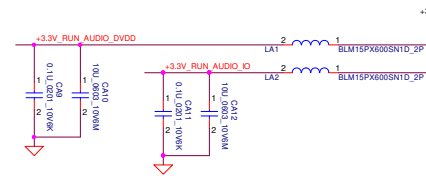
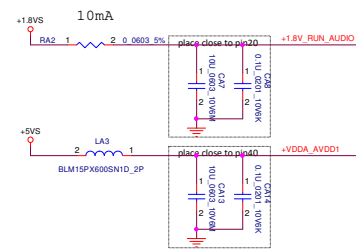
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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 54 of 121

Main Function:

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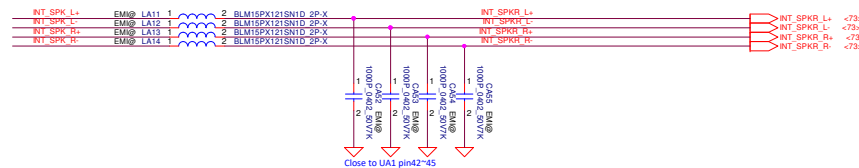
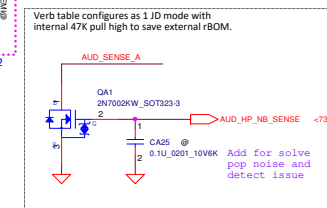
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Verbi table configures as 1D mode with internal 47k pull high to save external ROM.

EMI added 06/02

AUD\_SENSE\_A

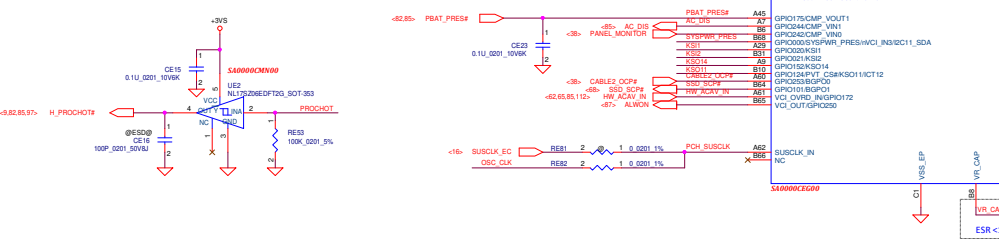
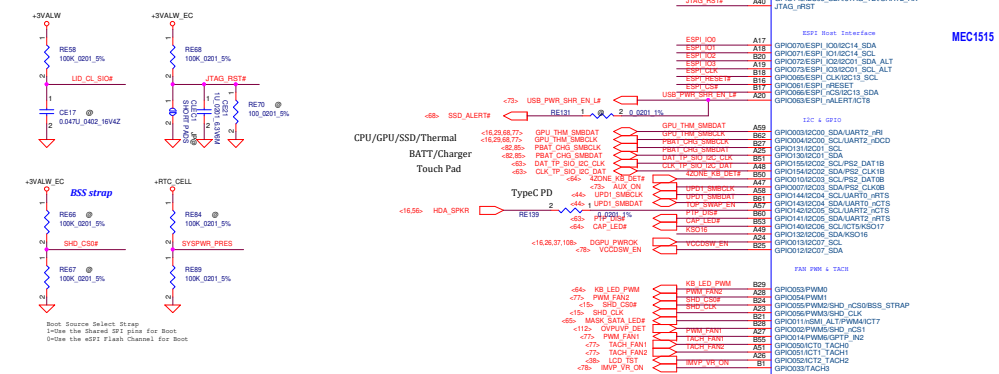
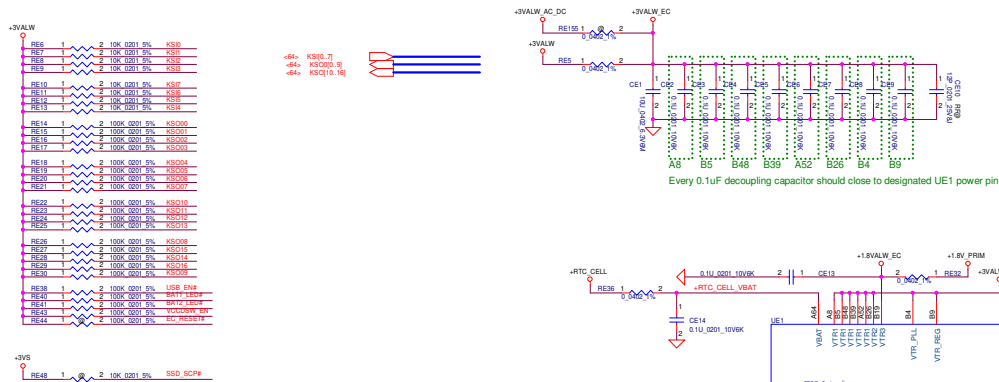




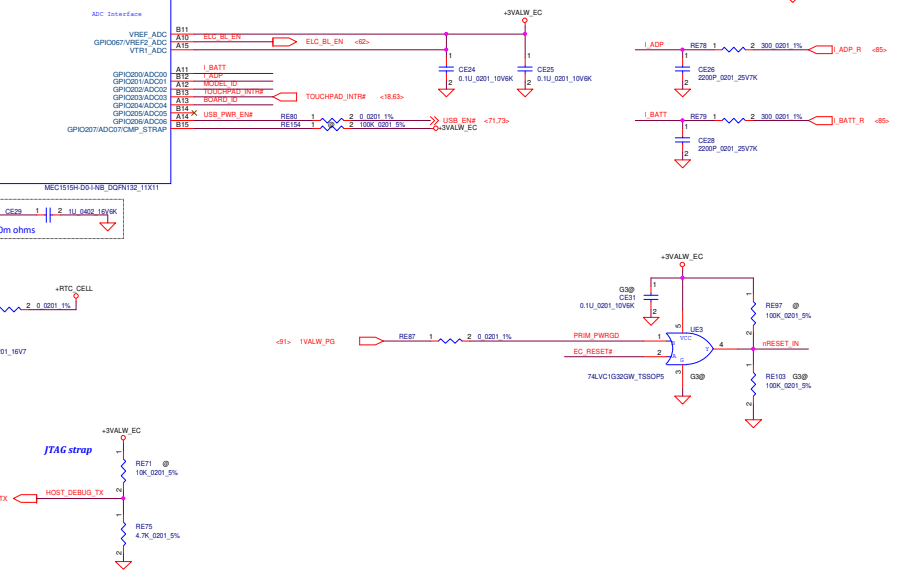
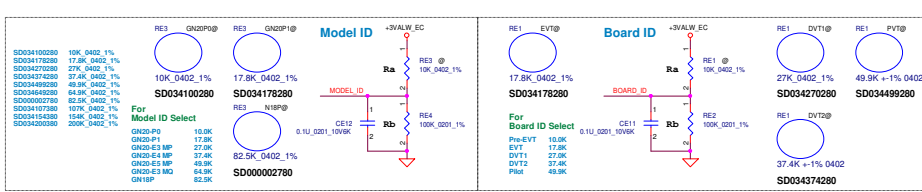
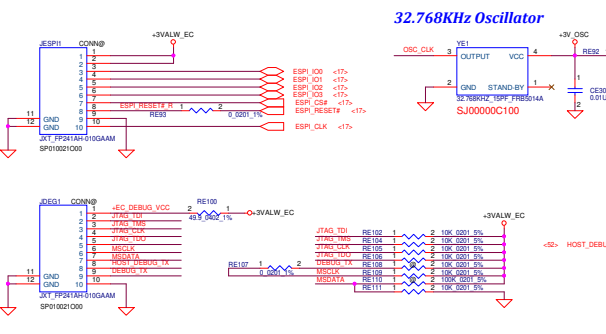
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Pin Name	Strap Name	Strap define and value	IO Power rail
GPI0170	JTAG_STRAP	1=Use the JTAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VTR1
GPI0104	VTR2_STRAP	Voltage Level strap is used to determine if the Shared Flash interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VTR1
GPI0045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keypower connector Note: This pin requires an external pull-up for normal operation.	VTR1
GPI0207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE (Hardware Default (GPIO input)) 1=Comparator 0 Enabled	VTR1
GPI0055/SHD_CS	BSS_STRAP	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VTR2
GPI0227/SHD_I2O	PWRG_STRAP	Primary Power rails good 1 = Primary power rails are good 0 = Primary power rails not stable	VTR2





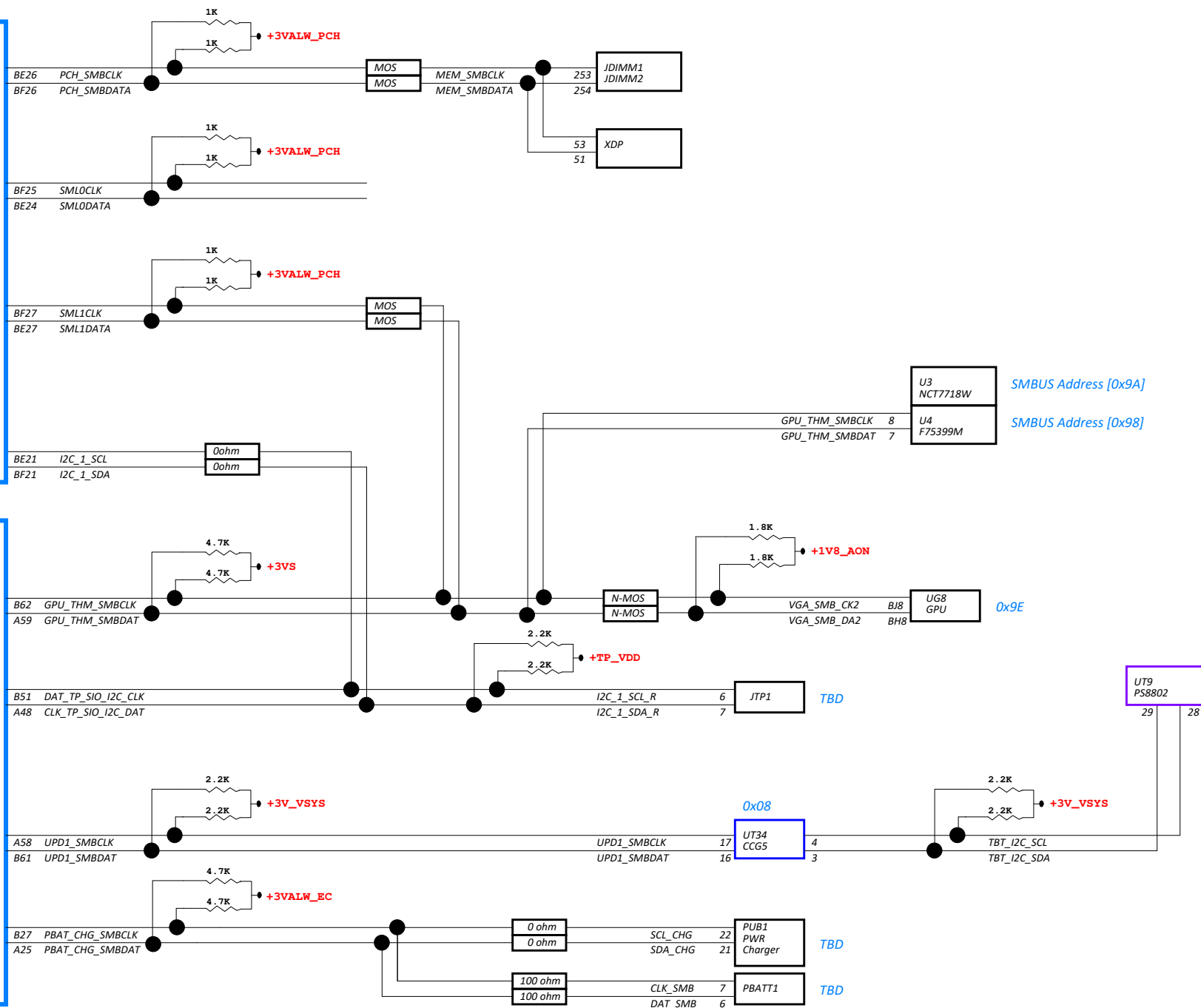
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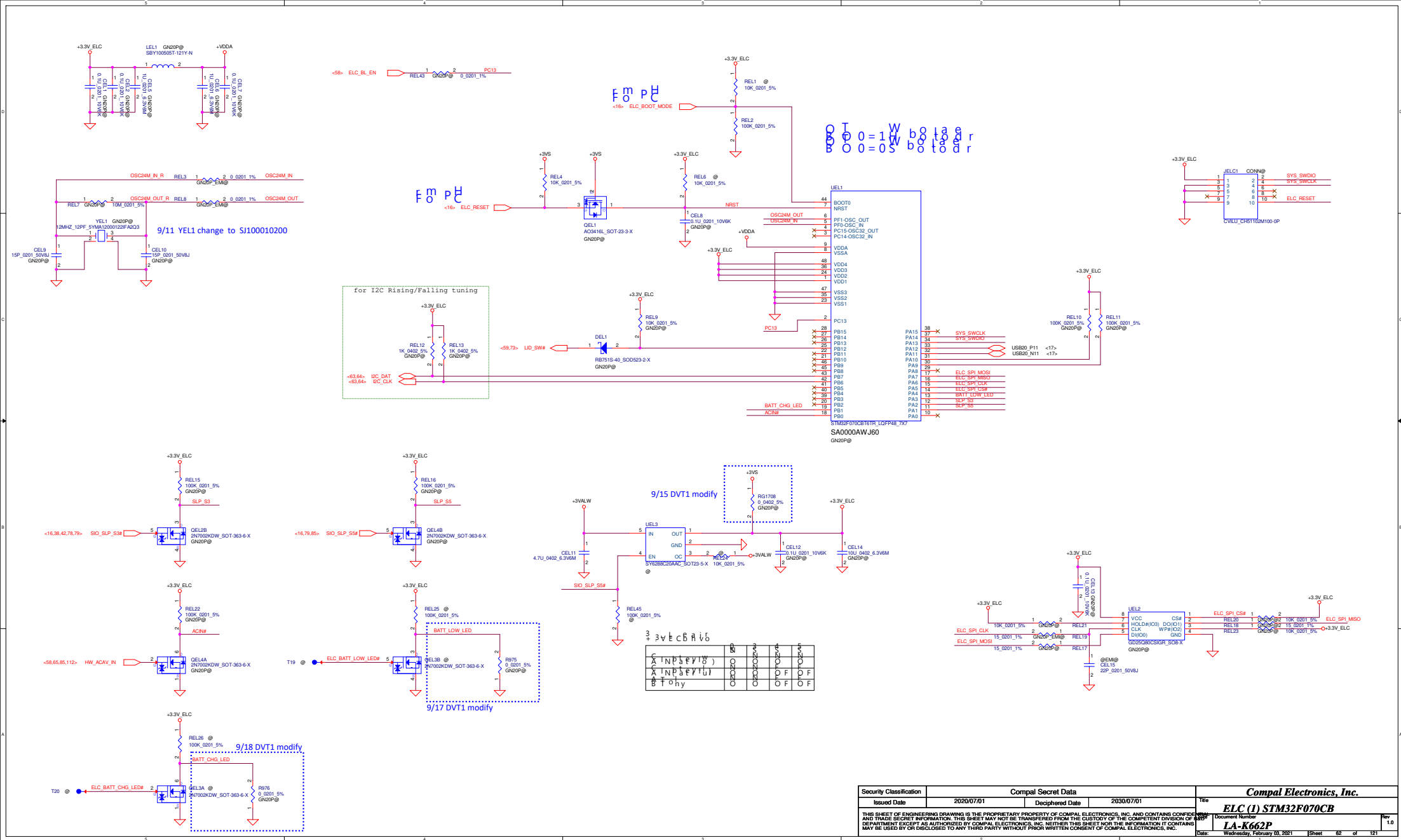
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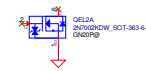


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Date:				Wednesday, February 05, 2021	Sheet 82 of 121

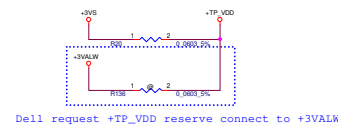
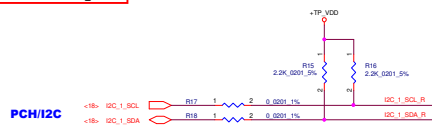
Main Func = ELC

Main Func = Power LED

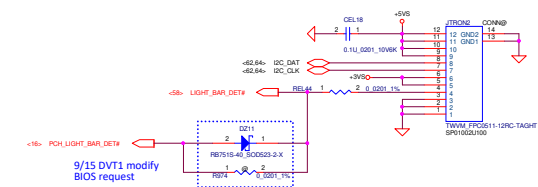
Main Func = ON/OFF TRON



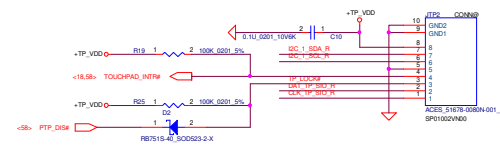
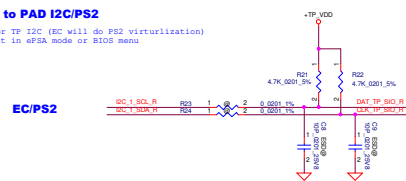
Main Func = Touch pad



Main Func = Primax Front Lighting

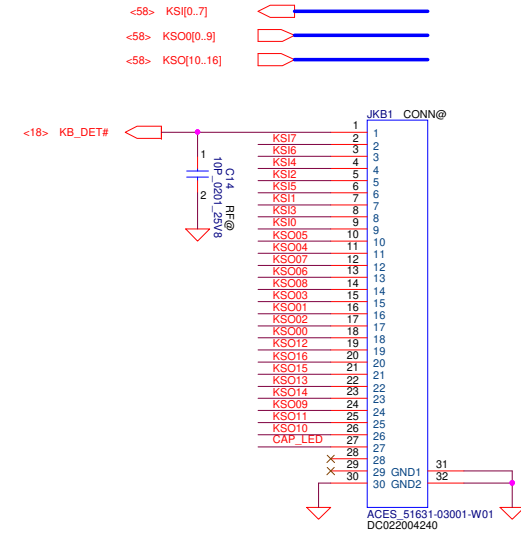
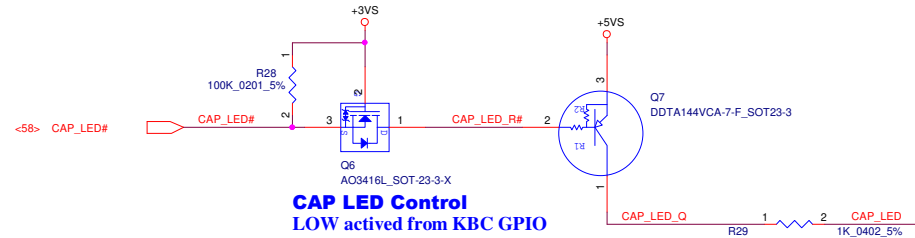


Co-lay EC to PAD I2C/PS2  
It's used for TP I2C (EC will do PS2 virtualization)  
as control it in ePSA mode or BIOS menu

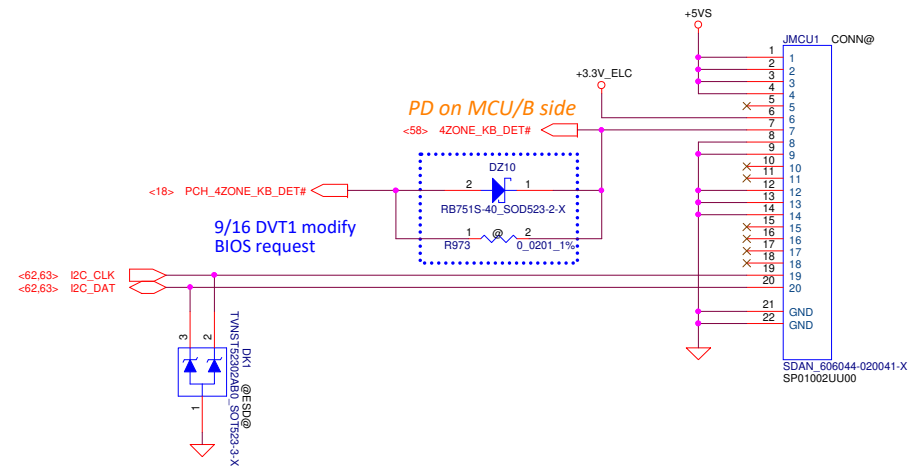
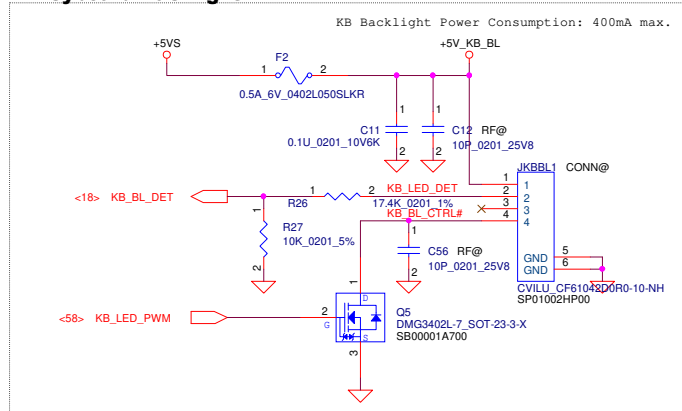


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Main Func = KB/KBBL



Keyboard Backlight



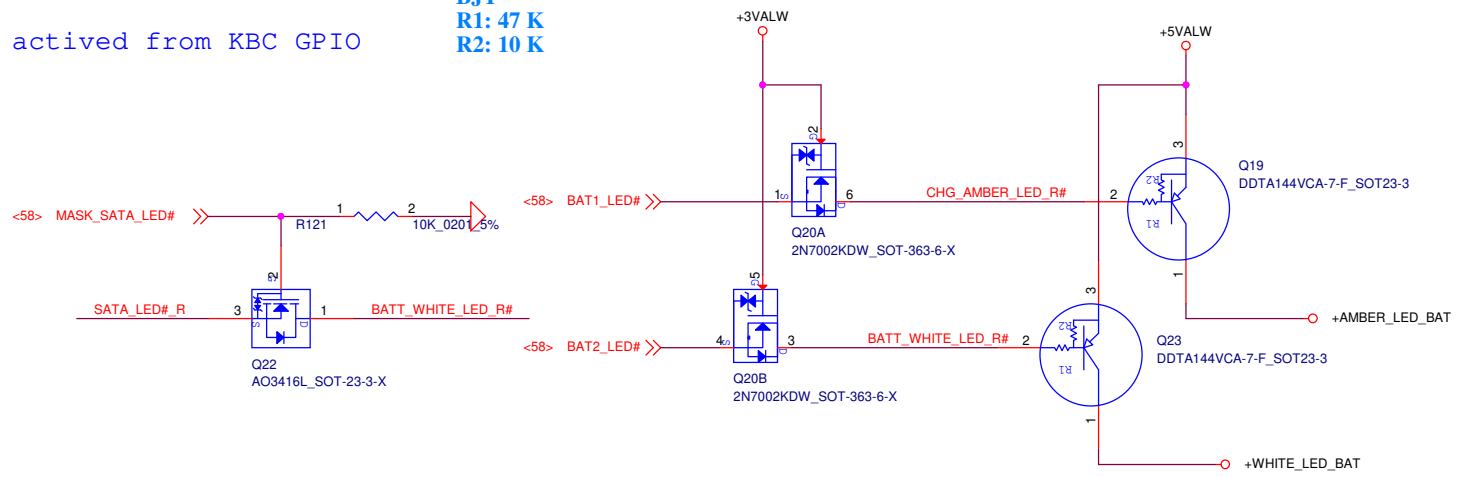
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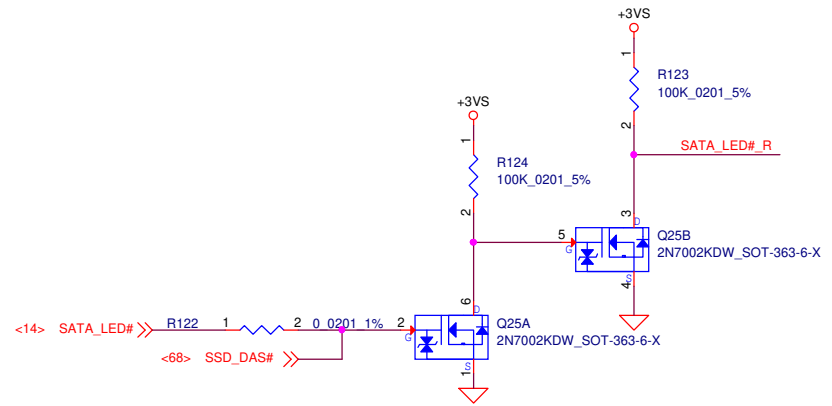
Main Func = Battery LED

Low active from KBC GPIO

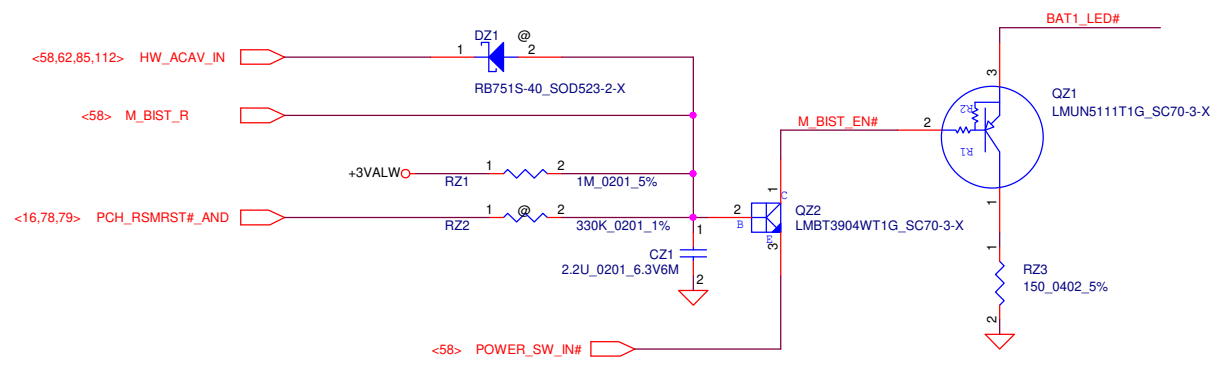
BJT  
R1: 47 K  
R2: 10 K



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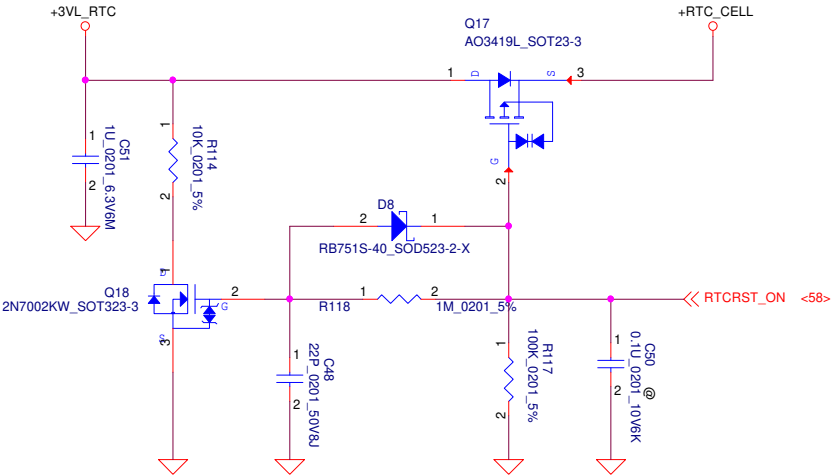


Main Func = M\_BIST



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				Rev	1.0

Main Func = RTC Gen9

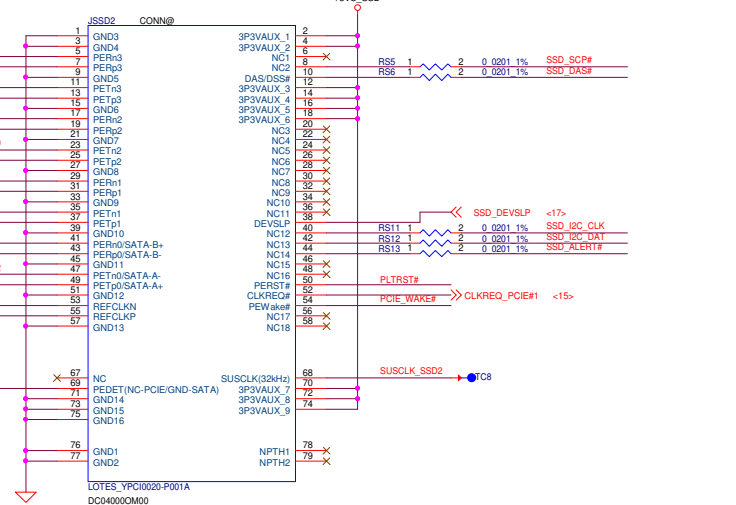
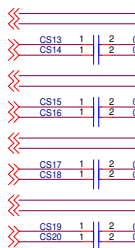
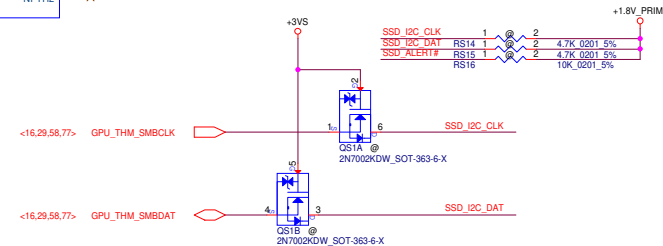
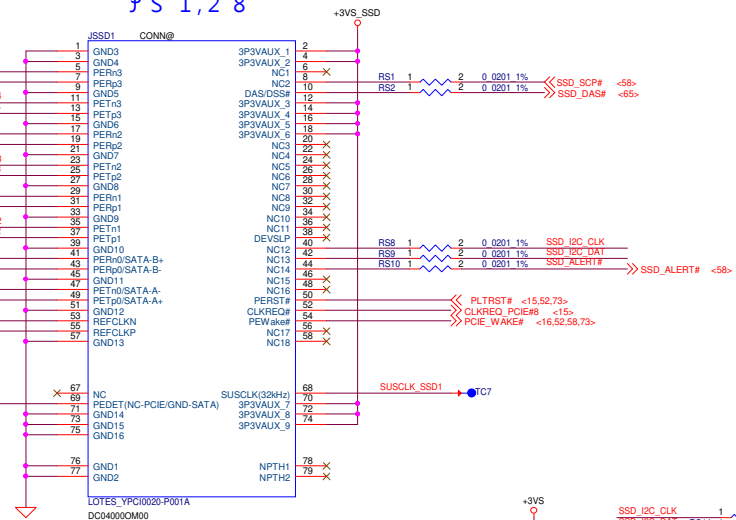
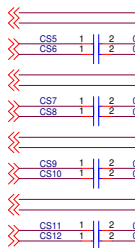
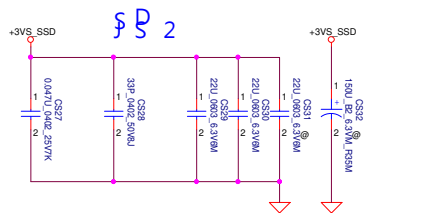


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				Date:	Wednesday, February 03, 2021
				Sheet	66 of 121
				Rev	1.0

Main Function:

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PEDET	Module Type
0	SATA
1	PCIe

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						Size	Document Number		Rev	
							<b>LA-K662P</b>		<b>1.0</b>	
Date:		Wednesday, February 03, 2021		Sheet	68	of 121				

Main Function:

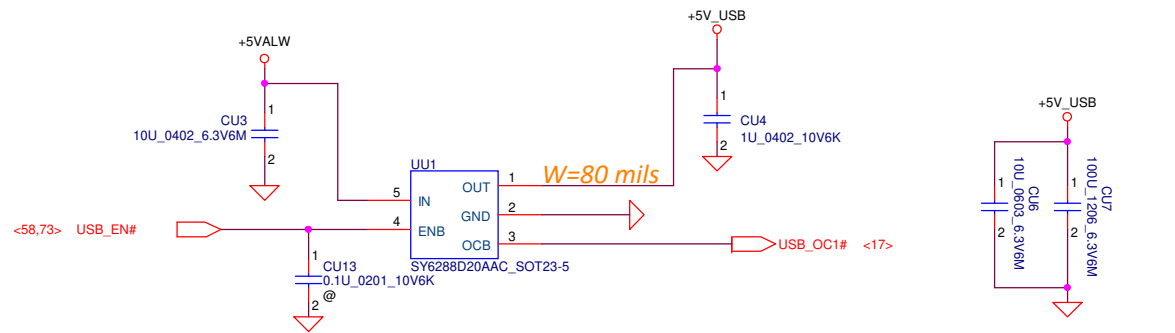
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					LA-K662P	1.0
				Date:	Wednesday, February 03, 2021	Sheet 69 of 121

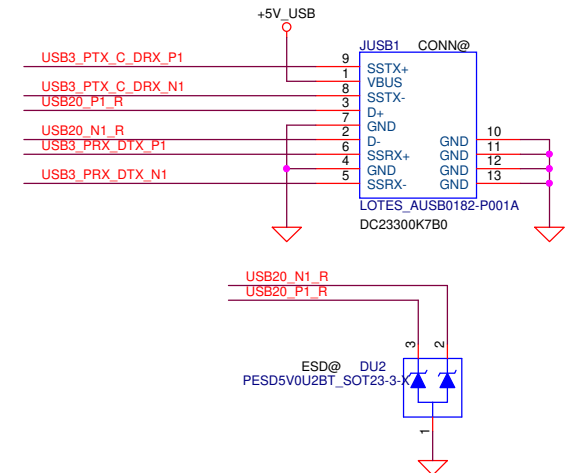
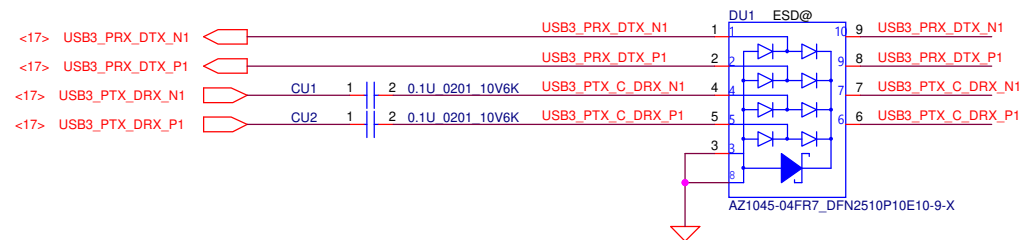
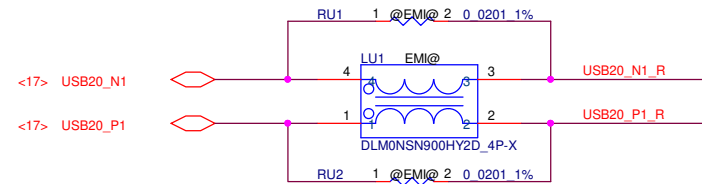
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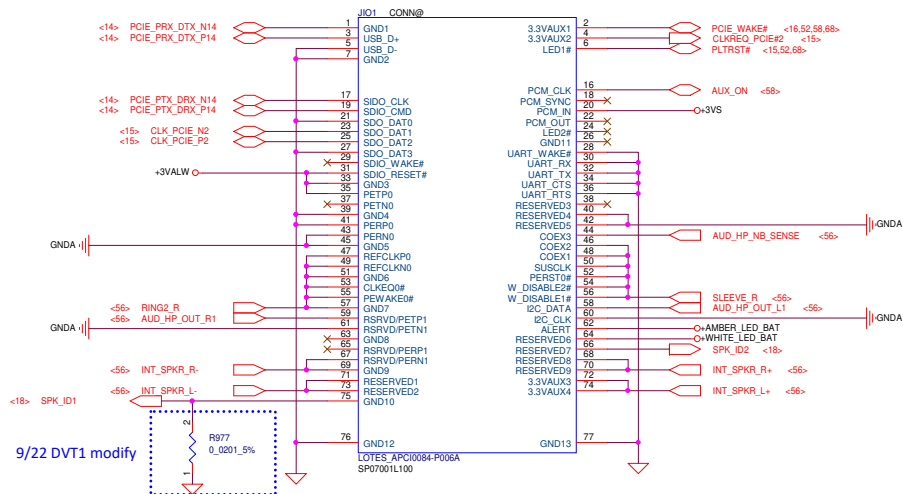
Main Function:

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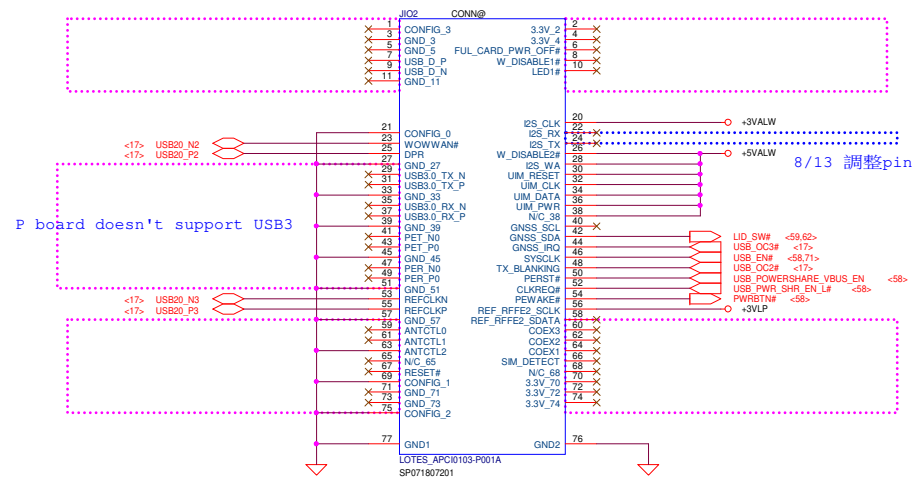


## A Key CONN

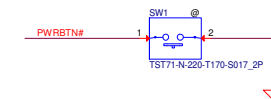


### For LAN DB CONN (LEFT)

## B Key CONN



### For USB DB CONN (RIGHT)



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				LA-K662P		Rev	1.0
				Date:	Wednesday, February 03, 2021	Sheet	73 of 121

Main Function:

Reserve

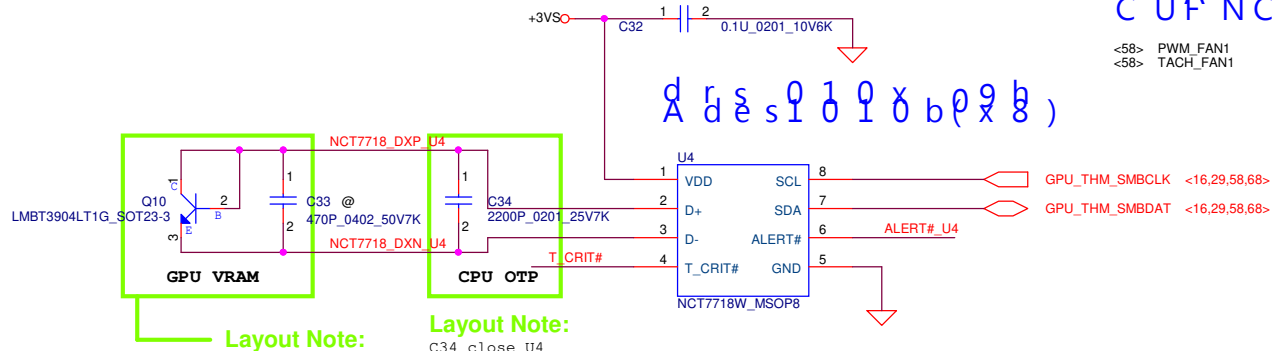
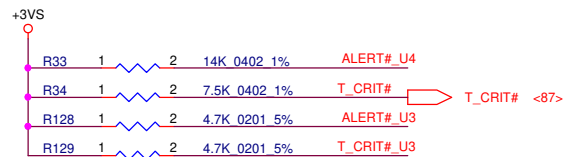
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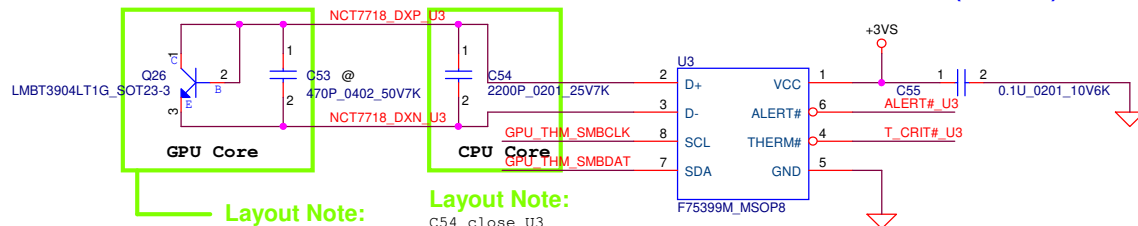
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Layout Note: DXN and DXP routing width and spacing is 10 mil / 10 mil.



Layout Note: DXN and DXP routing width and spacing is 10 mil / 10 mil.

TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

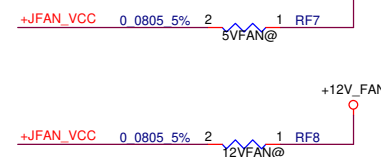
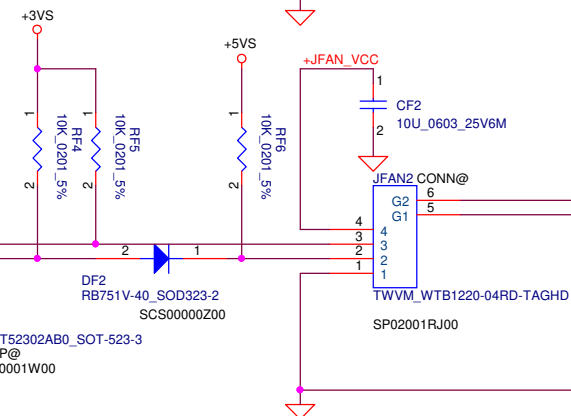
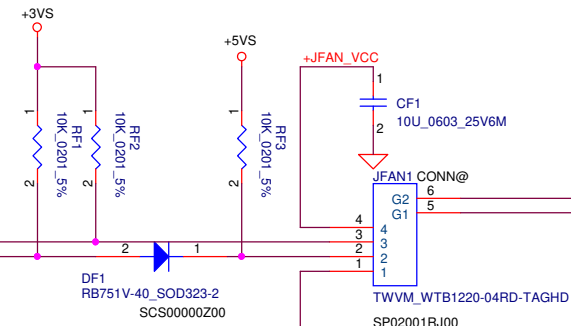
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Compal Secret Data

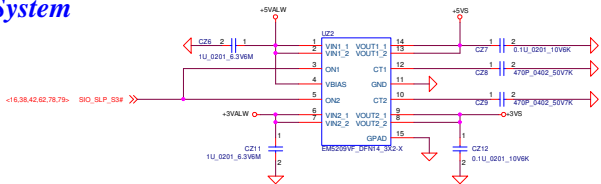
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<58> TACH\_FAN1

Compal Secret Data

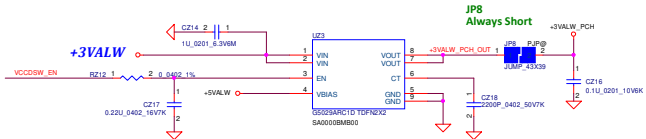
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<58> TACH\_FAN2



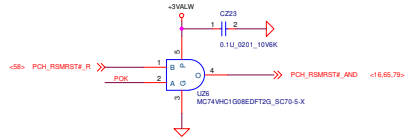
+5VS / +3VS for System



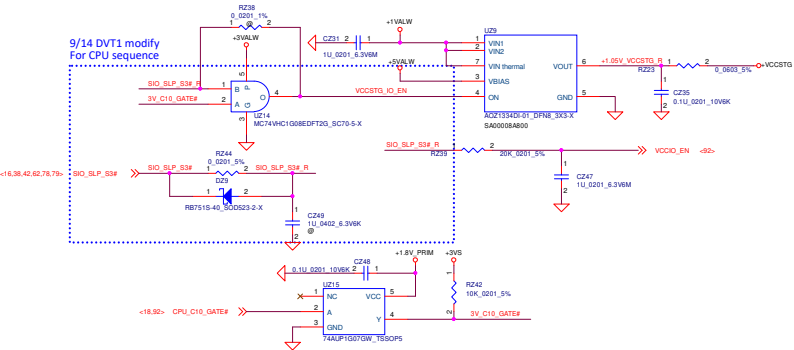
+3VALW TO +3VALW\_PCH



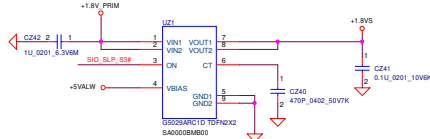
RSMRST circuit



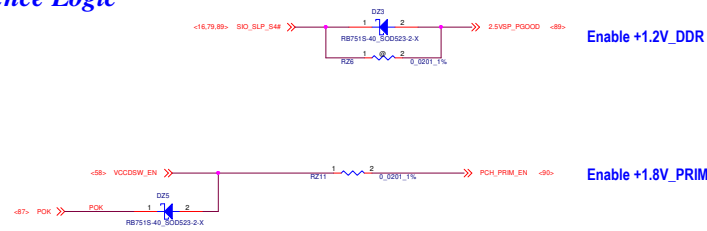
VCCSTG



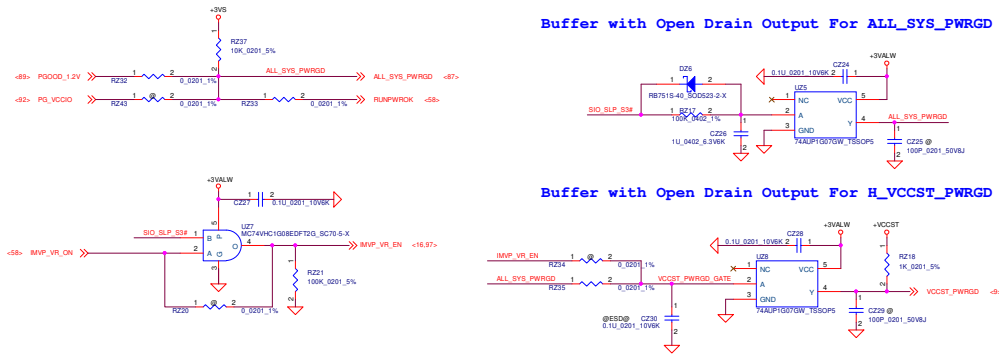
+1.8VS for System



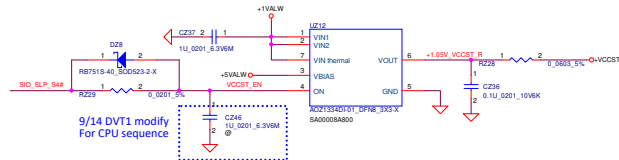
Sequence Logic



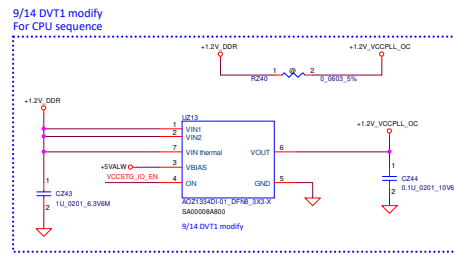
IMVP\_VR\_ON&VCCST\_PWRGD



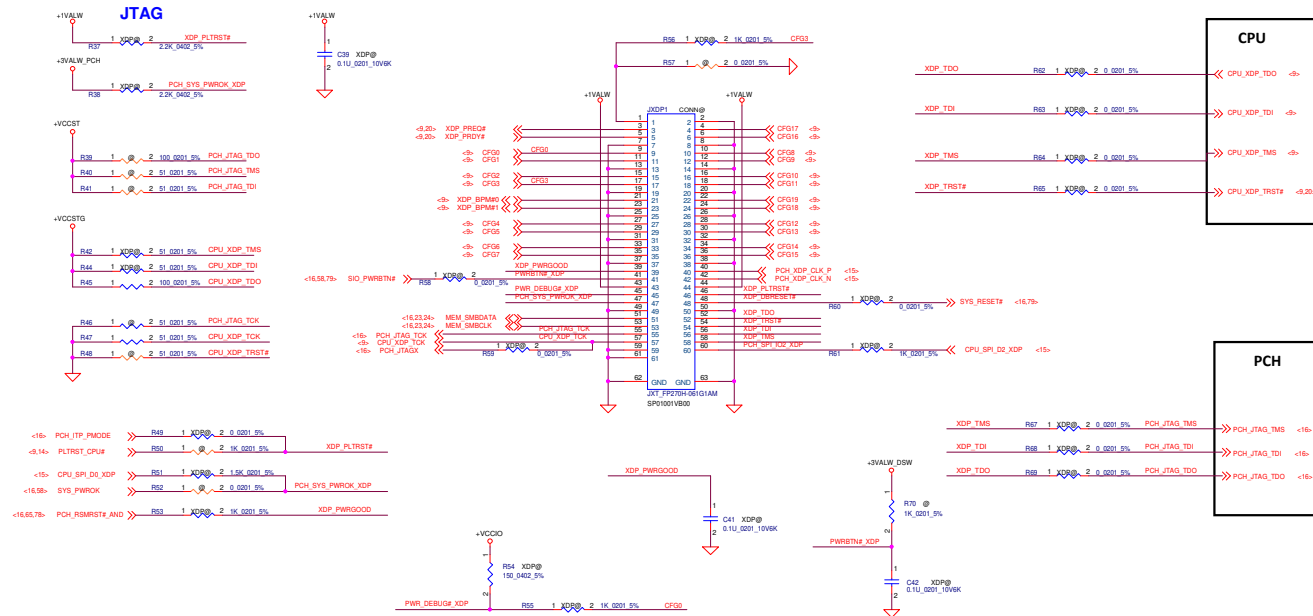
VCCST



VCCPLL\_OC

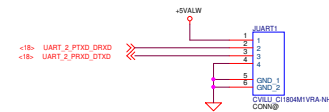


## XDP

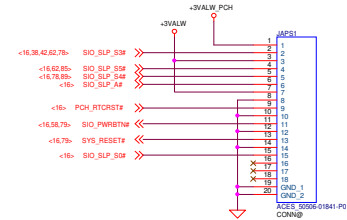


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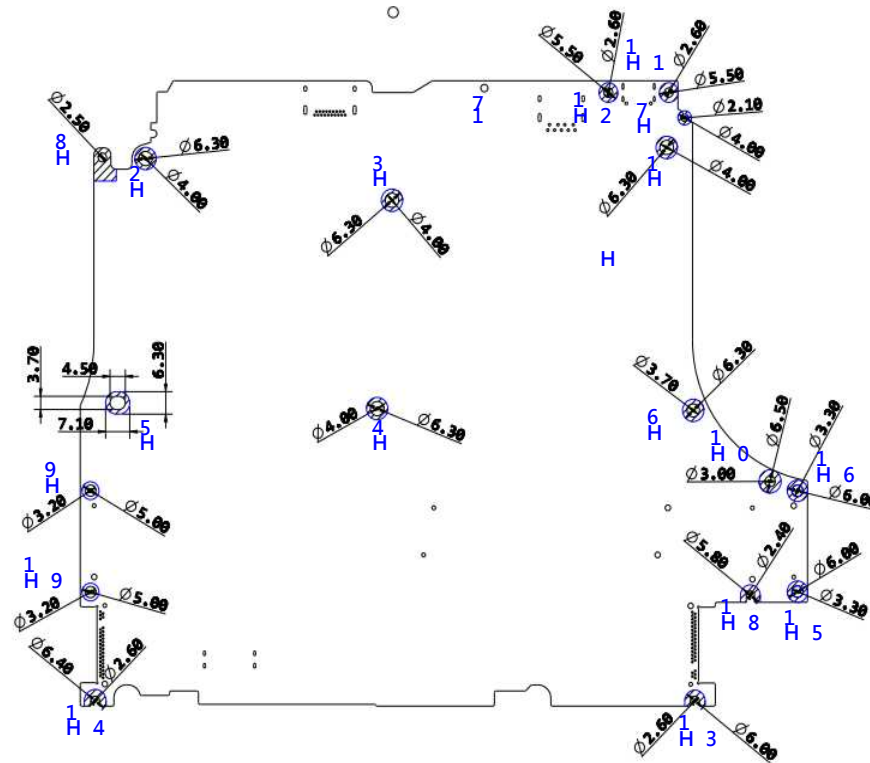
## BIOS UART Debug



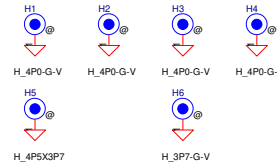
APS



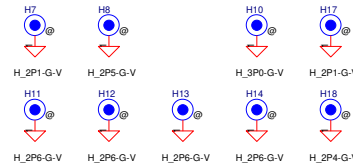
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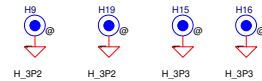
U & G U



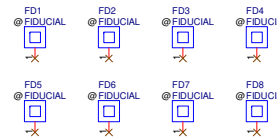
P H



g a d f



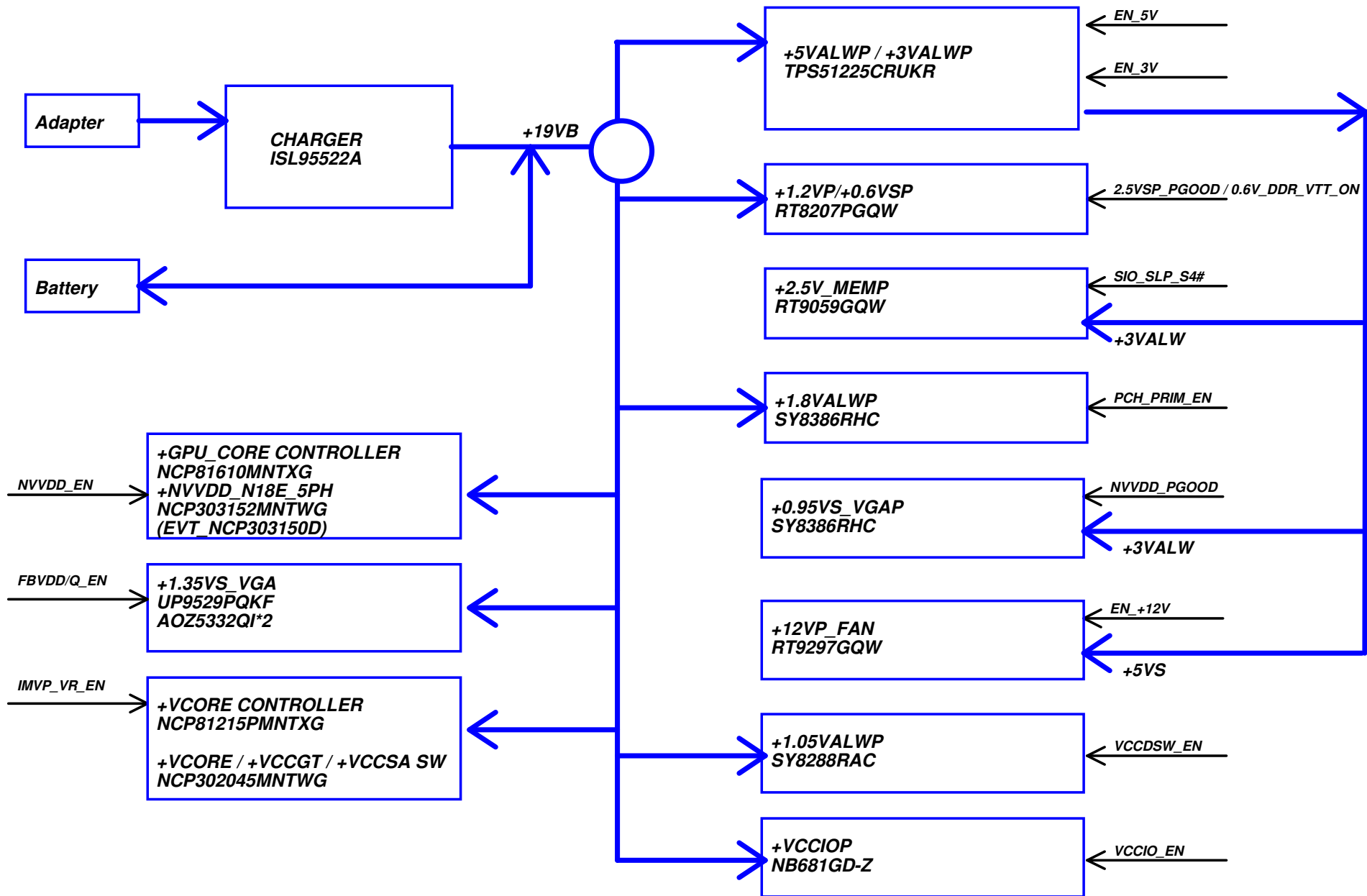
f d t a M a k



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# Power block



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# Main Func = DCIN CONN

## 20200915 Modify DCIN pin define Adapter Connector

Adapter Bot Side  
ACES\_SMB01001-P01  
PIN1 PSID  
PIN2 GND  
PIN3 GND  
PIN4 GND  
PIN5 GND  
PIN6 GND  
PIN7 GND  
PIN8 ADPIN  
PIN9 ADPIN  
PIN10 ADPIN  
PIN11 ADPIN  
PIN12 ADPIN  
PIN13 ADPIN  
ACES\_50493-01301-P01

Adapter 180W / 240W  
240W/19V~12.63A

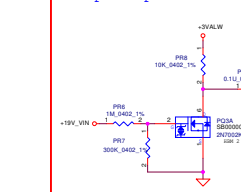
# Main Func = BATT CONN

## Battery Connector

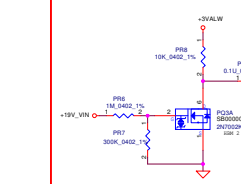
Battery Bot Side  
PIN1 BATT+  
PIN2 BATT+  
PIN3 BATT+  
PIN4 CLK\_SMB  
PIN5 DAT\_SMB  
PIN6 BATT\_PRES#  
PIN7 SYS\_PRES#  
PIN8 GND  
PIN9 GND  
PIN10 GND  
SP07001R500

Battery 56W  
56W/11.4V~4.91A  
Battery 86W  
86W/11.4V~7.54A

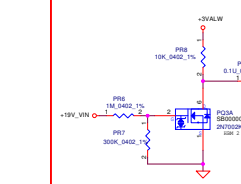
## Adapter protection:



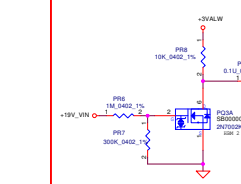
## Battery protection:



## +3VALW\_EC



## +3VLP +3.3V\_BAT\_LDO COIN RTC Battery



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Date				Drawn	1.0

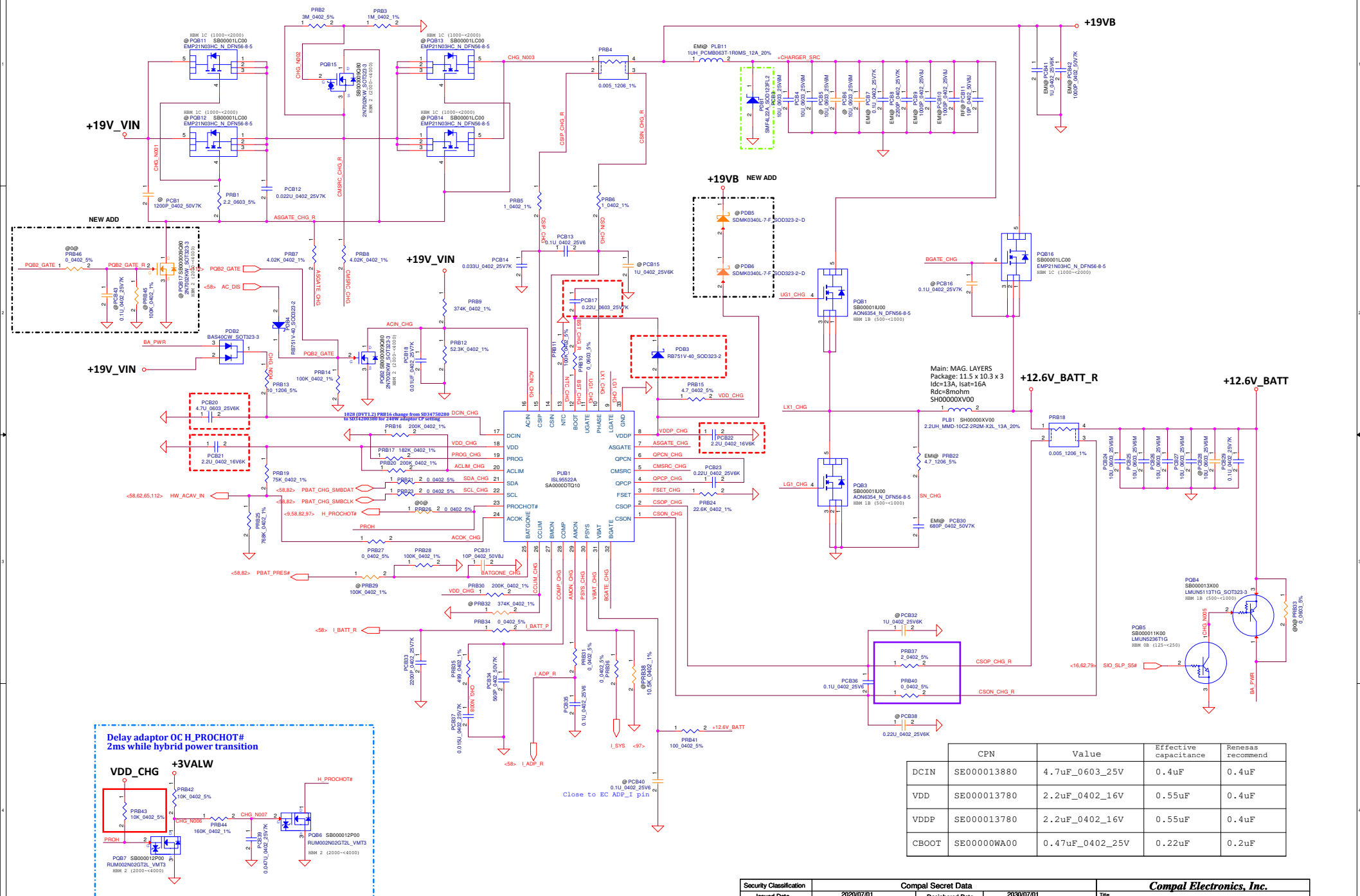
# Reserve for PWR

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# Reserve for PWR

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**Main Func = CHARGER**



	CPN	Value	Effective capacitance	Reenas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.55uF	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.22uF	0.2uF

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**Main Func = 3VALWP / 5VALWP**

Input Current: 14.06A  
 $3.4V \times 9.97A / 0.85 / 9V = 4.43A$   
 $5.16V \times 14.28A / 0.85 / 9V = 9.63A$

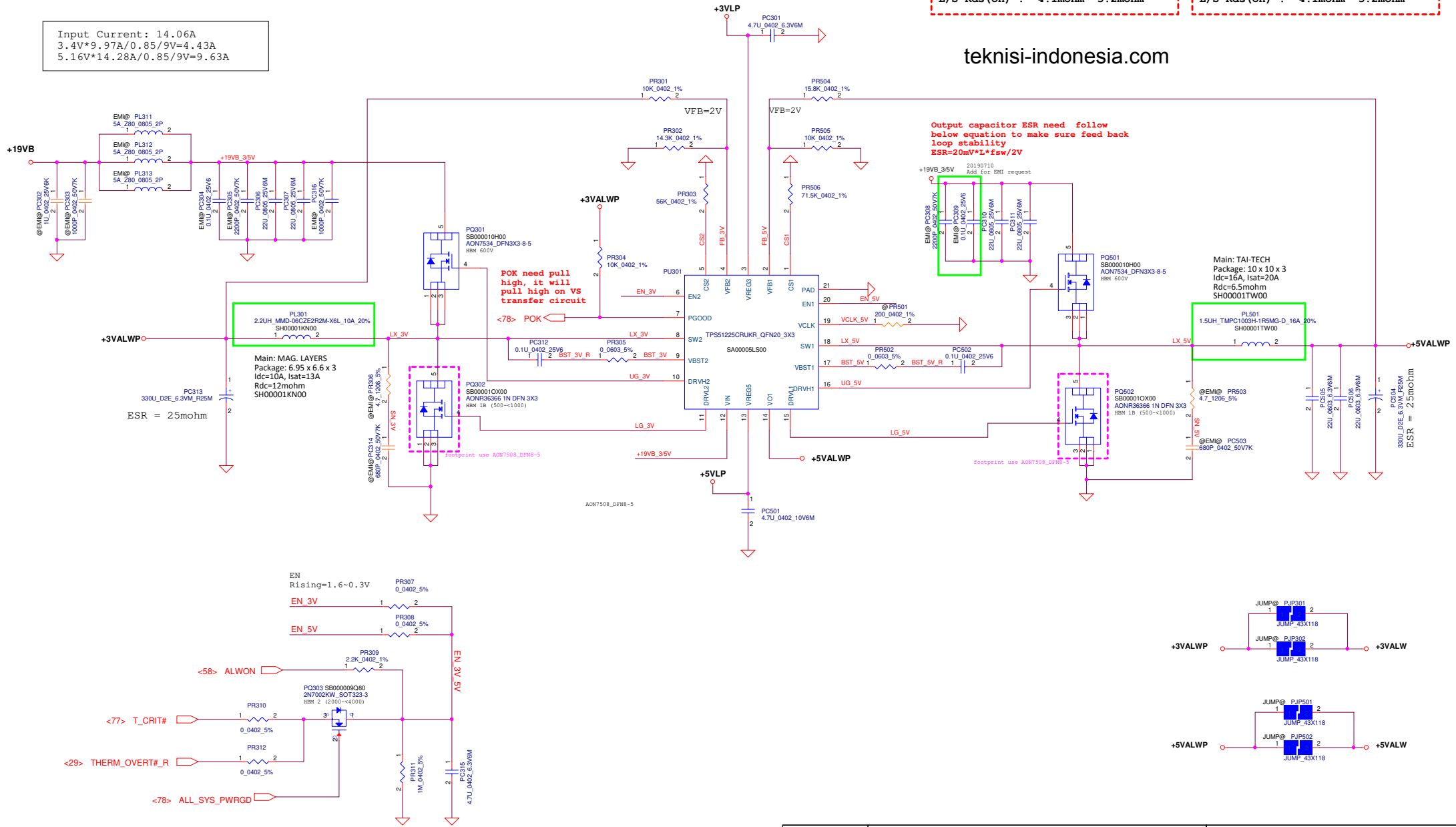
```
3VALWP
Vout=3.4V
TDC 10A
Peak Current 11.5A
OCP current 13 A
OVP=3.824V~3.994V(112.5%~117.5%)
UVP=1.869V~2.209V(55%~65%)
FSW=355kHz
```

MOS (VGS = 4.5V )		
	TYP	MAX
H/S Rds (on) :	6.7mohm	8.5mohm
L/S Rds (on) :	4.1mohm	5.2mohm

5VALWP  
Vout= 5.16V  
TDC 14.5A  
Peak Current 17.7A  
OCP current 20A  
OVP=5.805V~6.063V(112.5%~117.5%)  
UVP=2.838V~3.354V(55%~65%)  
FSW=300KHz

MOS (VGS = 4.5V )		
	TYP	MAX
H/S Rds (on) :	6.7mohm	8.5mohm
L/S Rds (on) :	4.1mohm	5.2mohm

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# Main Func = 1.2VP / 0.6VSP / 2.5V\_MEMP

Input Current: 1.012A

1.203V\*5.92A/0.85/9V=0.93A

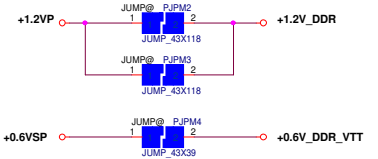
0.6V\*1.05A/0.85/9V=0.082A

Pin19 need pull separate from +1.2VP.  
If you have +1.2V and +0.6V sequence question,  
you can change from +1.2VP to +1.2VS.

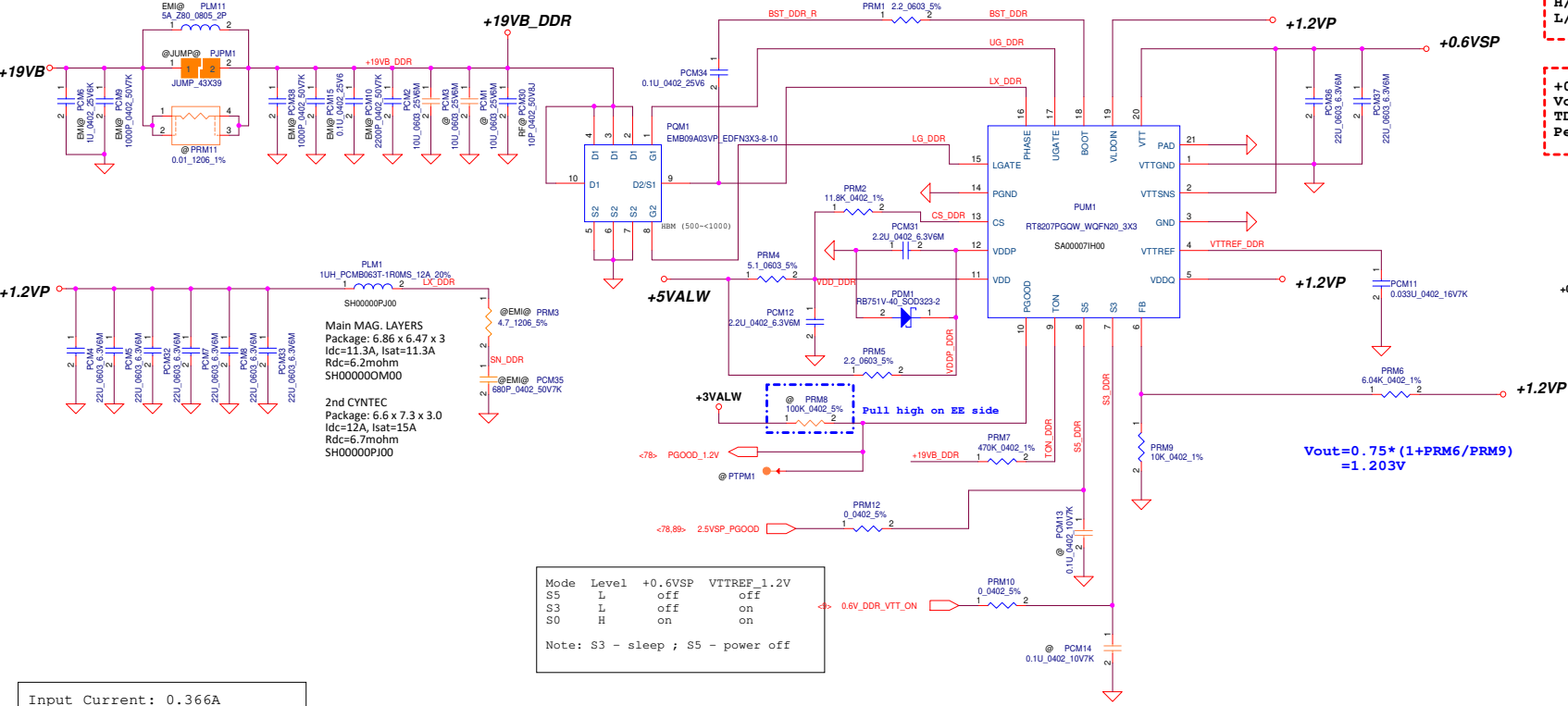
+1.2VP  
Vout= 1.203V  
TDC 5.35A  
Peak Current 7.64A  
OCP current 10.12A  
OVP=1.36V~1.44V (113%~120%)  
UVP=0.72V~0.96V (60%~80%)  
FSW= ~538 Hz

MOS (VGS = 4.5V )  
TYP MAX  
H/S Rds (on) : 11mohm 13mohm  
L/S Rds (on) : 11mohm 13mohm

+0.6VSP  
Vout= 1.203V  
TDC 1A  
Peak Current 1.5A



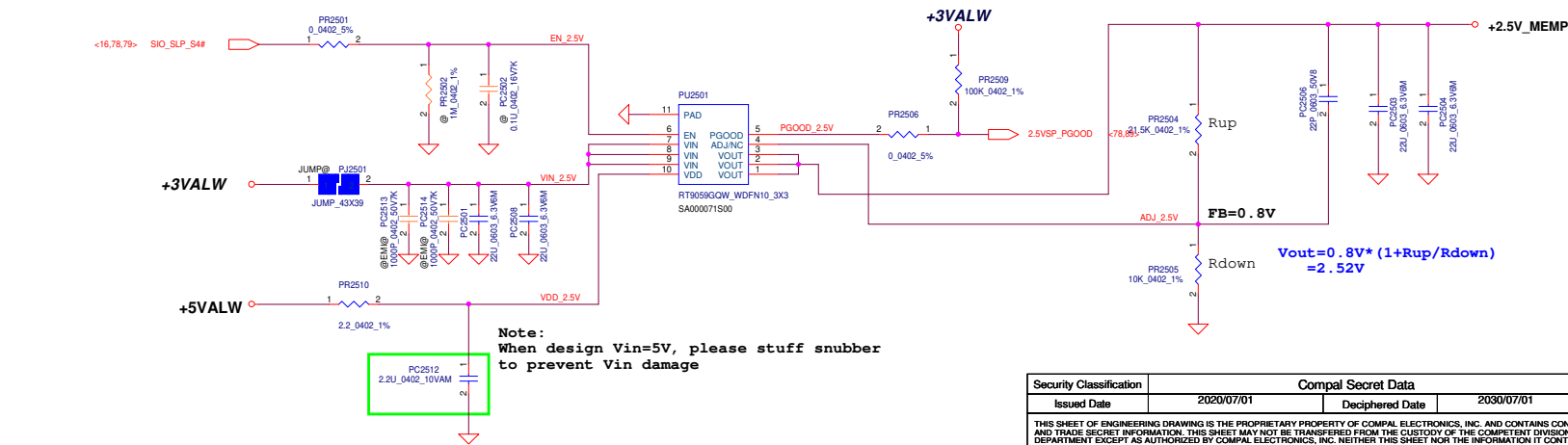
+2.5V\_MEMP  
Vout= 2.52 V  
TDC 0.37 A  
Peak Current 0.528 A  
Current limit 3.6A



Input Current: 0.366A

2.52V\*0.37A/0.85/3V=0.366A

Mode Level +0.6VSP VTTREF 1.2V  
S5 L off off  
S3 L off on  
S0 H on on  
Note: S3 - sleep ; S5 - power off



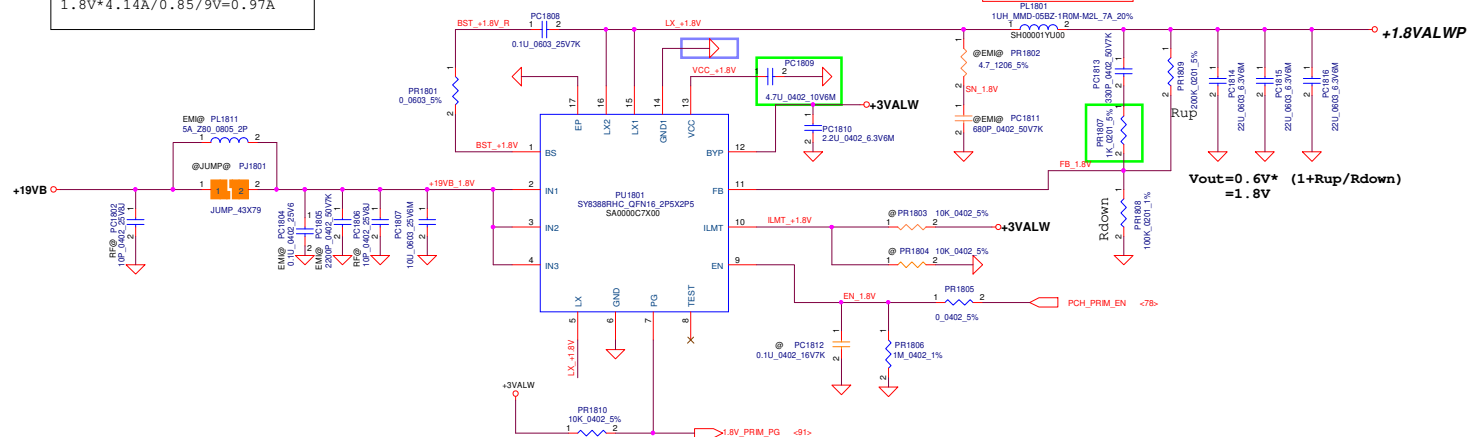
Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

**Main Func = 1.8VALWP**

Input Current: 0.97A  
 $1.8V \cdot 4.14A / 0.85 / 9V = 0.97A$

Main MAG. LAYERS  
Package: 5.49 x 5.18 x 2  
Idc=7A, Isat=13A  
Rdc=20mohm  
SH00001YU00

```
+1.8VALWP
TDC 3.64A
Peak Current 5.2A
Current limit 8A
OVP=2.106V~2.214V(117%~123%)
UVP=0.99V~1.17V(55%~65%)
FSW= 500K Hz
```

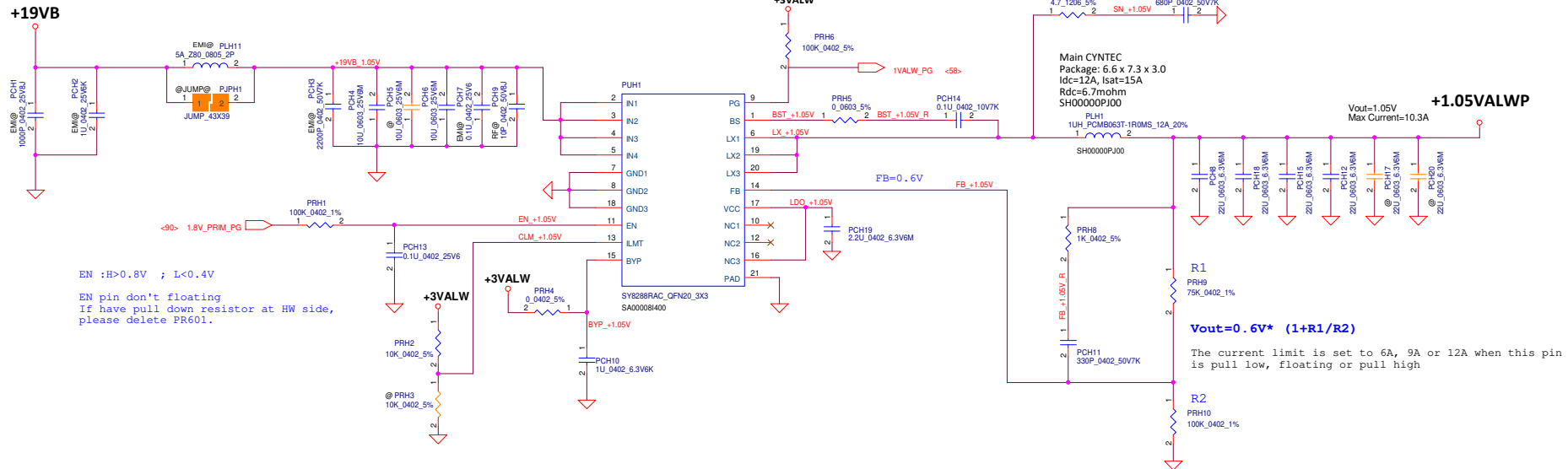


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Main Func = 1.05VALWP

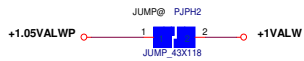
Input Current: 0.97A  
 $1.05V \times 4.8A / 0.85 / 9V = 0.66A$

+1.05VALWP  
 TDC 4.8A  
 Peak Current 6.85A  
 Current limit 8.22A  
 OVP=1.208V~1.313V (115%~125%)  
 UVP=0.63V~0.735V (60%~70%)  
 FSW= 500K Hz



EN :H>0.8V ; L<0.4V  
 EN pin don't floating  
 If have pull down resistor at HW side,  
 please delete PR601.

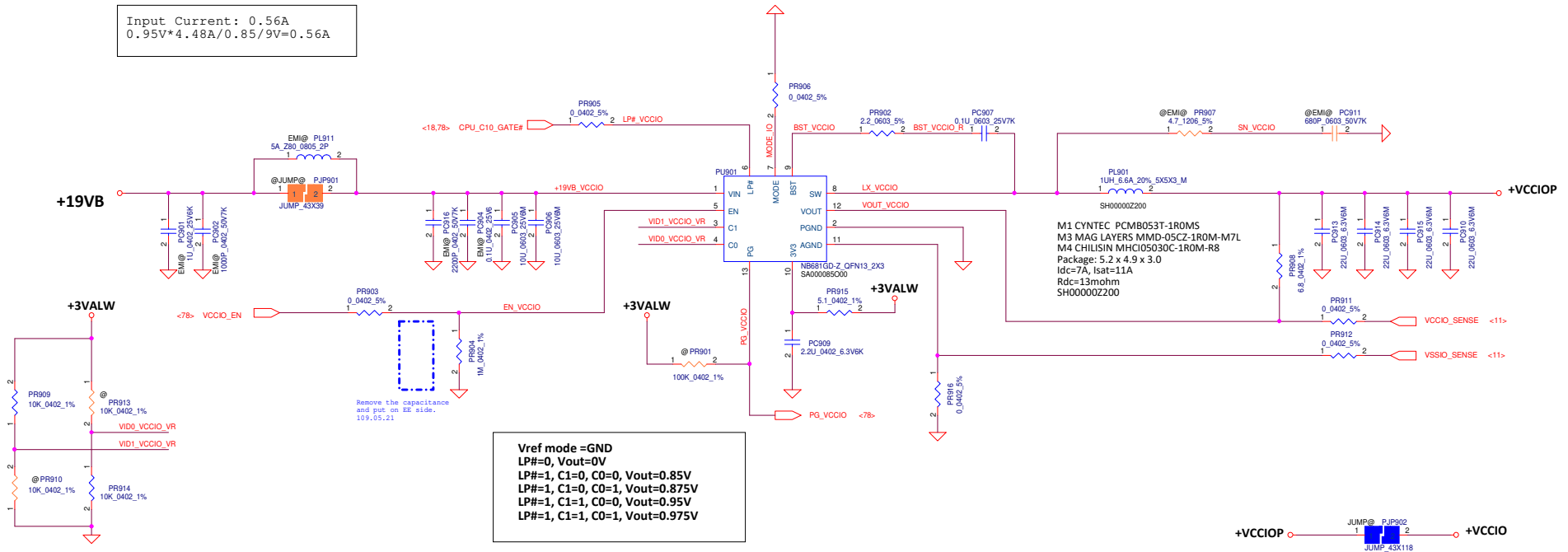
OCP setting	ILMT(pin13)
8A	Pull low
12A	Floating
16A	Pull high



**Main Func = +VCCIOP**

```
+VCCIOP (0.95V)
TDC 4.48A
Peak Current 6.4A
Current limit 7.6A
OVP=1.14V~1.28V(120%~135%)
UVP=0.665V~0.76V(70%~80%)
FSW= 750K Hz
```

Input Current: 0.56A  
 $0.95V \cdot 4.48A / 0.85 / 9V = 0.56A$



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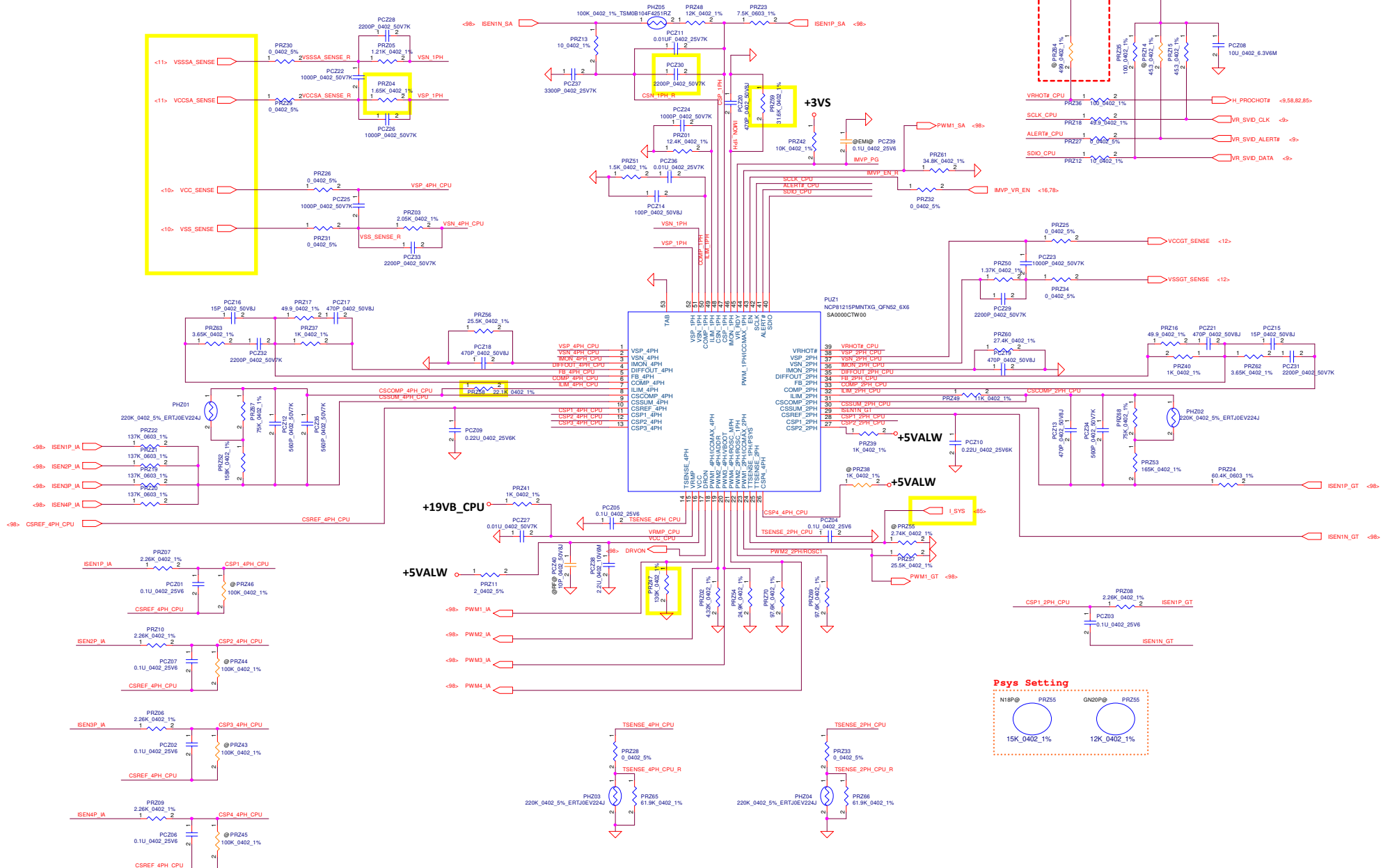
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Main Func = VCORE

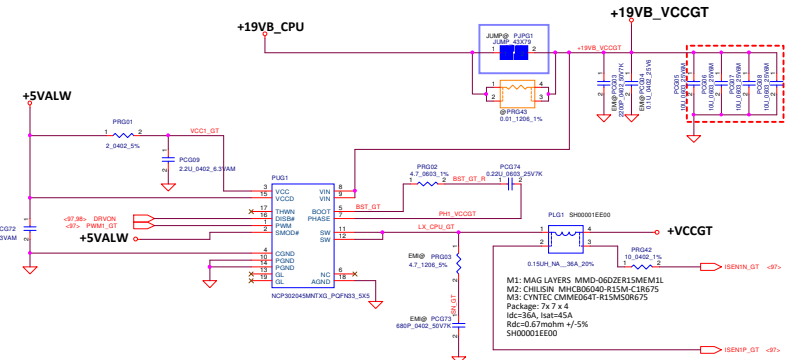
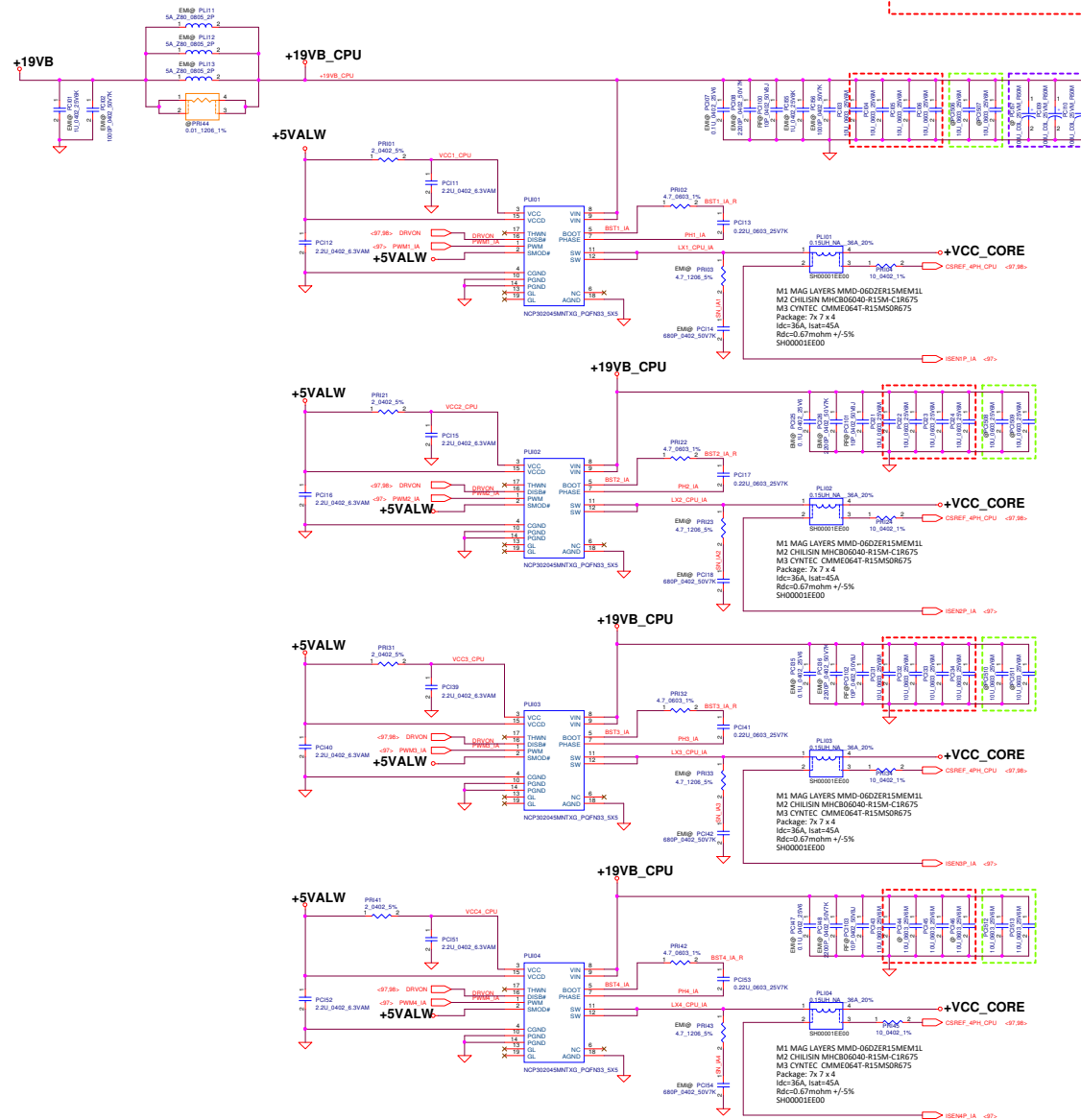
9/16 modify by Dell Dean



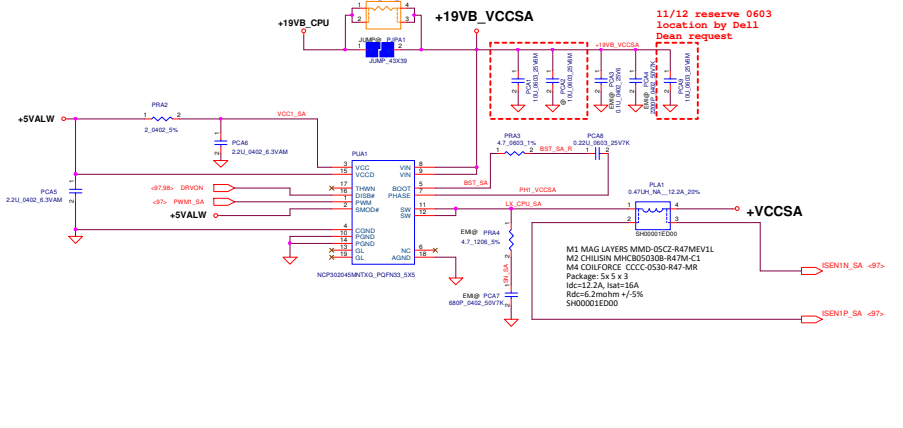
Main Func = CPU\_CORE\_SW

+VCC\_CORE  
TDC 125A  
Peak Current 165A  
Loadline 1.1mV/A

+VCCGT  
TDC 25 A  
Peak Current 32 A  
Loadline 2.7mV/A



+VCCSA  
TDC PL2 :10A  
Peak Current 11.1A  
Loadline 10.3mV/A



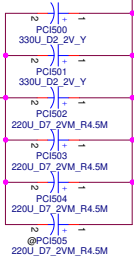
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PWR +VCC CORE		Rev
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Reserve for PWR

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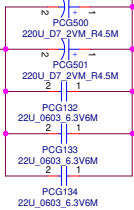
+VCC\_CORE



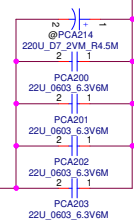
+VCC\_CORE  
470uF\_D2 x3  
220uF\_D7 x3  
47uF\_0603 x33  
10uF\_0402 x32  
1uF\_0201 x45

+VCCGT\_CORE\_Hel1a  
220uF\_D7 x2  
22uF\_0603 x13  
10uF\_0402 x10  
1uF\_0201 x12

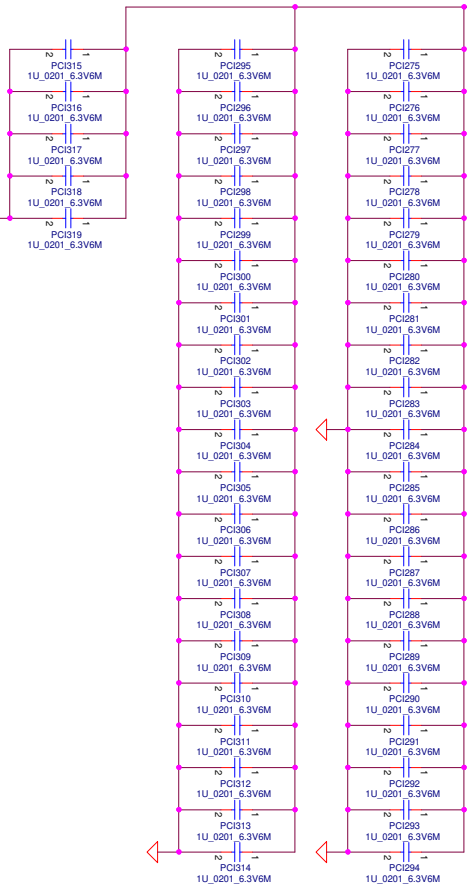
+VCCGT



+VCCSA



+VCCSA  
220uF\_D7 x1  
22uF\_0603 x6  
10uF\_0402 x7  
1uF\_0201 x1



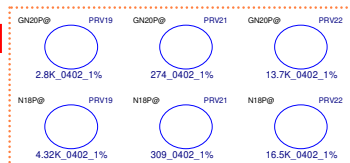
Security Classification	Issued Date	Comptel Secret Data	Declassified Date	2030/07/01	Title	Comptel Electronics, Inc.
2020/07/01	2030/07/01	PWR CPU DECOUPLING	LA-1743P	1.0	W:\electronics\cpu\decoupling\LA-1743P	101 of 181

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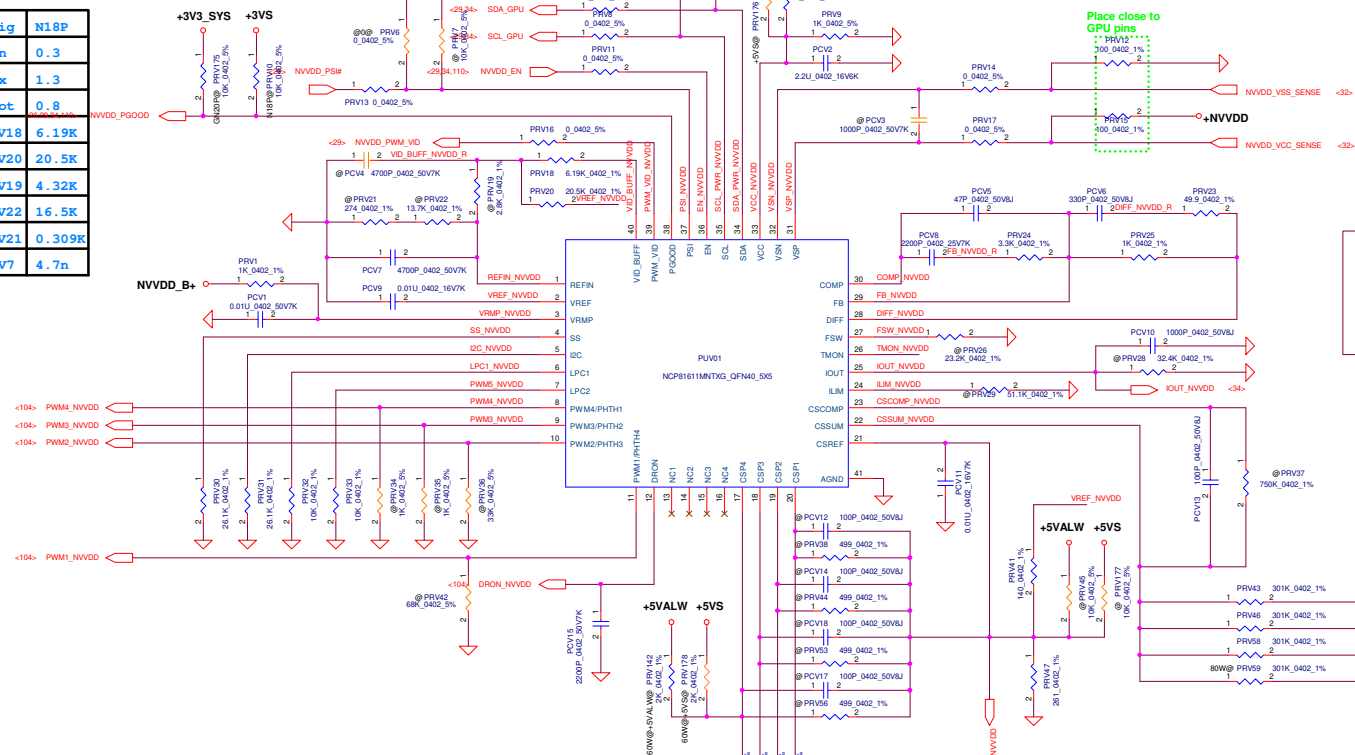
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**Main Func = VGA CORE**

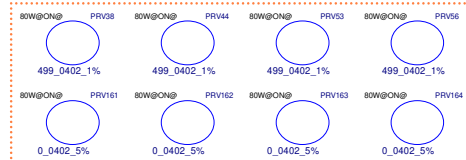
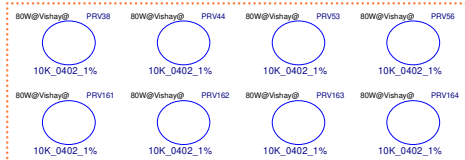
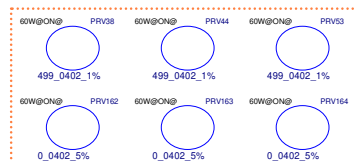
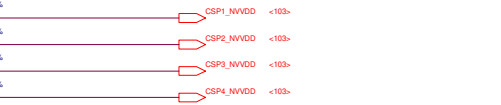
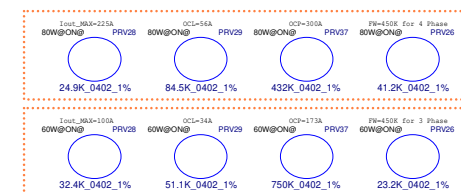
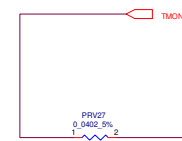
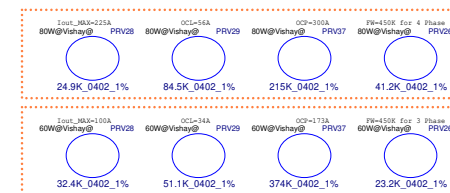


Config	GN20P	Config	N18P
Vmin	0.3	Vmin	0.3
Vmax	1.3	Vmax	1.3
Vboot	0.75	Vboot	0.8
R1=PRV18	6.19K	R1=PRV18	6.19K
R2=PRV20	20.5K	R2=PRV20	20.5K
R3=PRV19	2.8K	R3=PRV19	4.32K
R4=PRV22	13.7K	R4=PRV22	16.5K
R5=PRV21	0.274K	R5=PRV21	0.309K
C=PCV7	4.7n	C=PCV7	4.7n



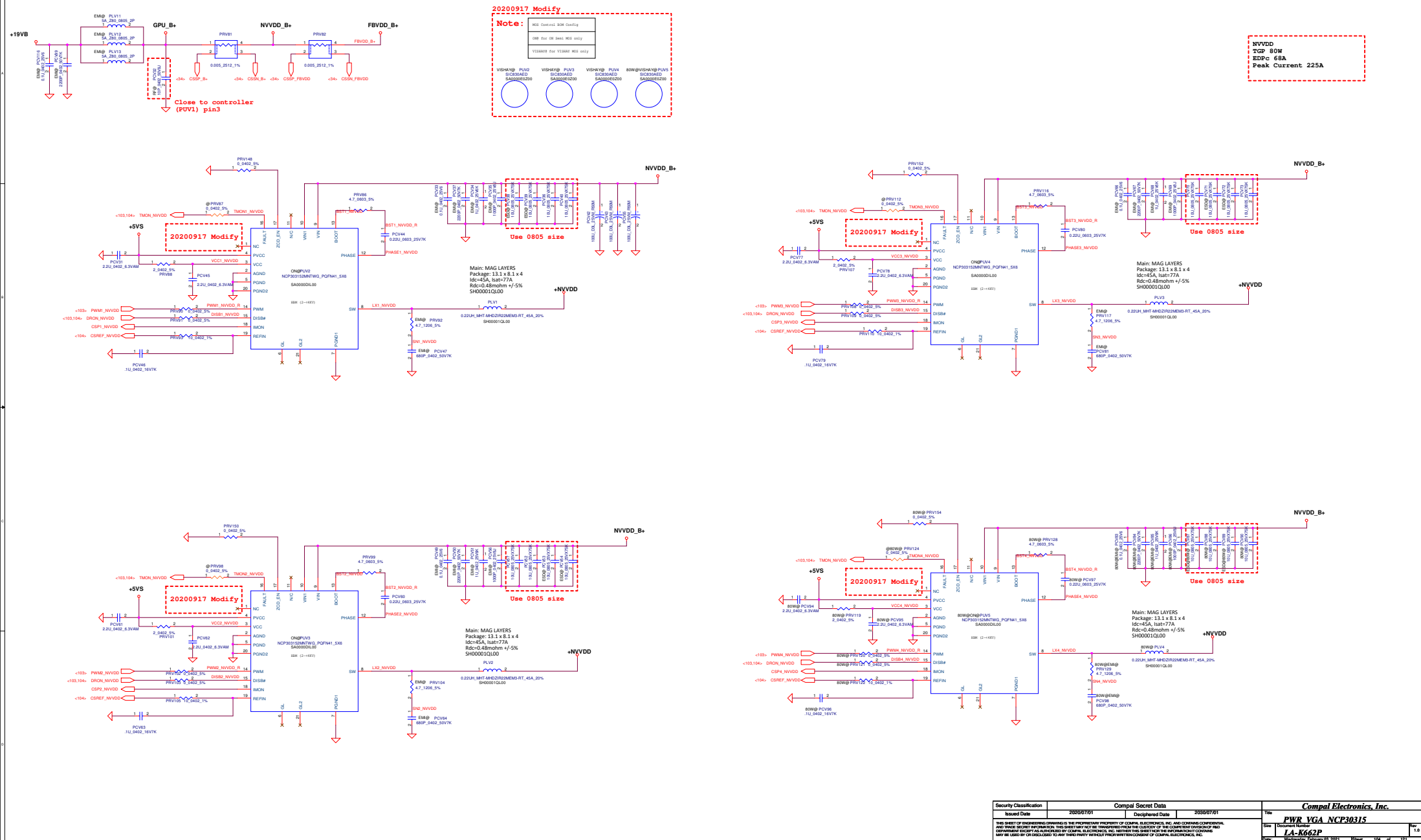
```
NVVDD - N18P
TGP 60W
EDPc 54.3A
Peak Current 99.2A
OCP 173A
OCL 34A
Freq 450K
```

NVVDD - GN20P  
TGP 80W  
EDPc 68A  
Peak Current 225A  
OCP 300A  
OCL 56A  
Freq 450K



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			<b>PWR VGA NCP81611MNTXG</b> <b>LA-R662P</b>	

Main Func = GPU\_CORE SW(1-4PH)





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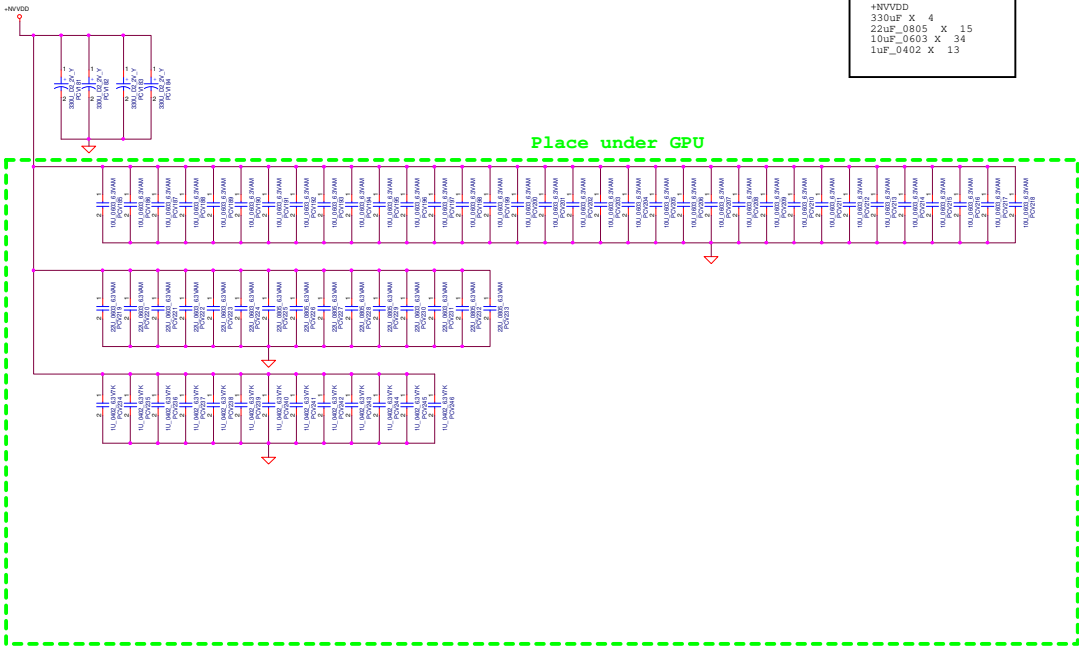
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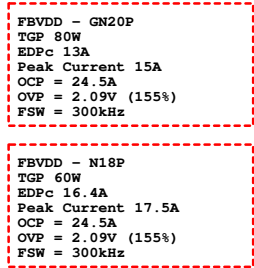
Main Func = VGA CORE DECOUPLING

+NVVDD  
330uF X 4  
22uF\_0805 X 15  
10uF\_0603 X 34  
1uF\_0402 X 13

Place under GPU



**Main Func =+FBVDDQ**



teknisi-indonesia.com

Main: MAG LAYERS  
Package: 6.86 x 6.47 x 4  
Idc=32A, Isat=55A  
Rdc=0.98mohm +/-5%  
SH00001G400

BOM config	GPU type	VRAM memory	VRAM vender	RVL	PRW30	PRW31
	GN20E			1.25V	16.9K	
				1.2V	16.9K	133K

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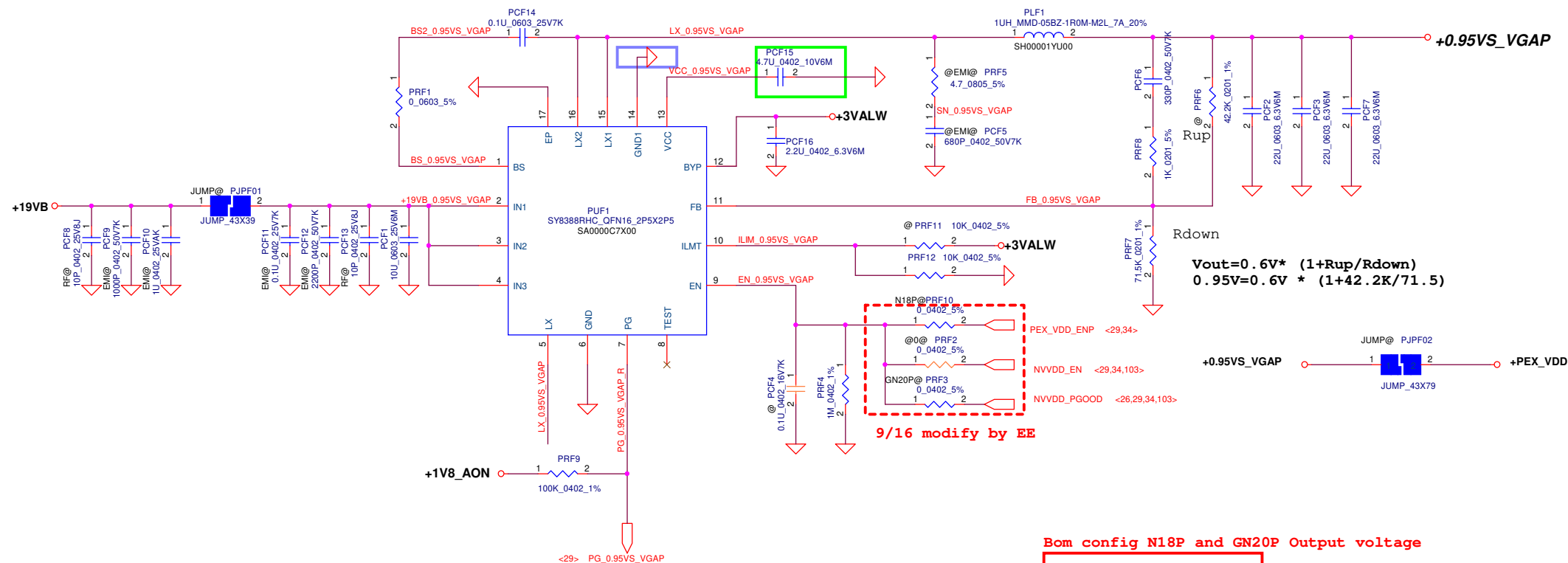
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# Main Func =+0.95VS\_VGAP

Input Current: 0.974A  
0.954V\*2.604A/0.85/3V=0.974A

Main MAG. LAYERS  
Package: 5.49 x 5.18 x 2  
Idc=7A, Isat=13A  
Rdc=20mohm  
SH00001YU00

+0.95VS\_VGAP  
TDC 2.3A  
Peak Current 3A  
OCP Current 6A fix by IC  
Fsw=1MHz



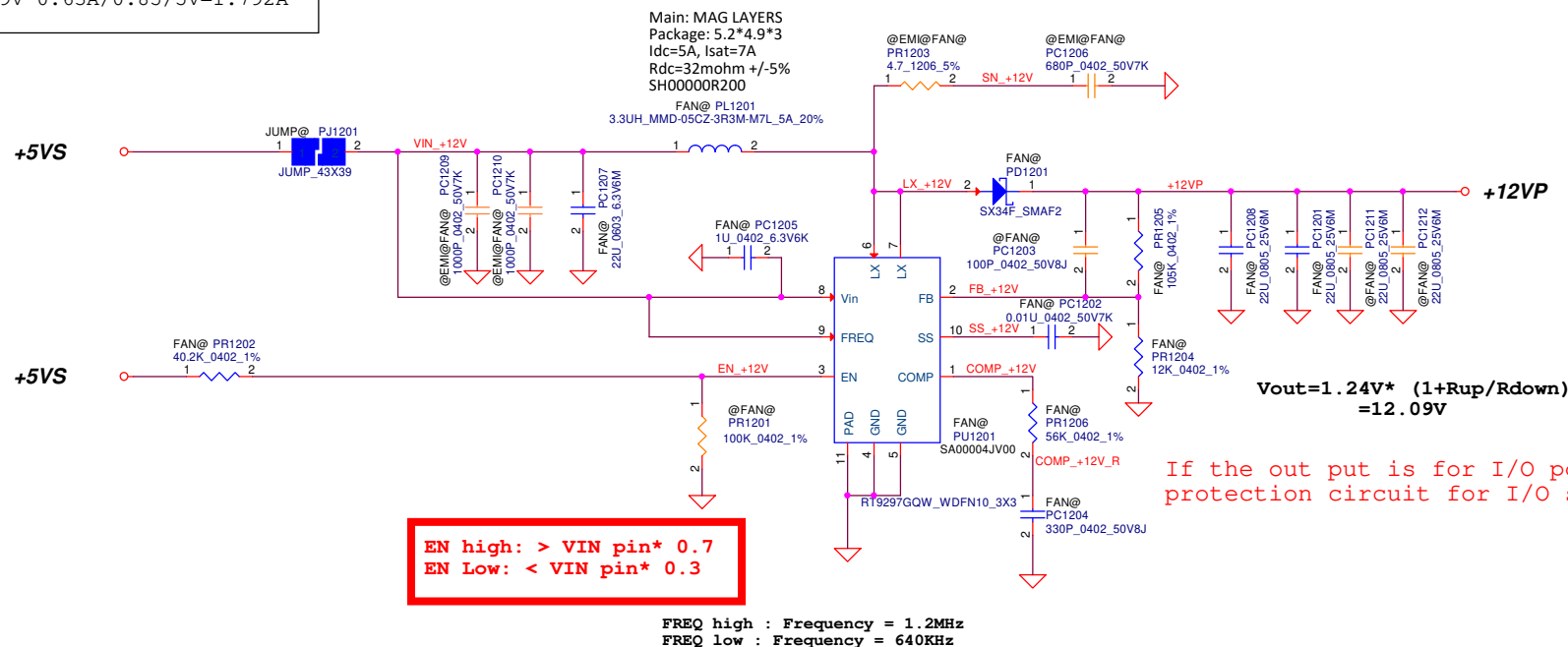
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# Main Func =+12VP\_FAN

+12VP  
Vout = 12.09 V  
TDC 0.63A  
Peak Current 0.9A  
Current limit 3A (input)  
FSW=1.24MHz

Add a switch circuit to turn off the +12V\_VIN if need.

Input Current: 1.792A  
 $12.09V \times 0.63A / 0.85 / 5V = 1.792A$

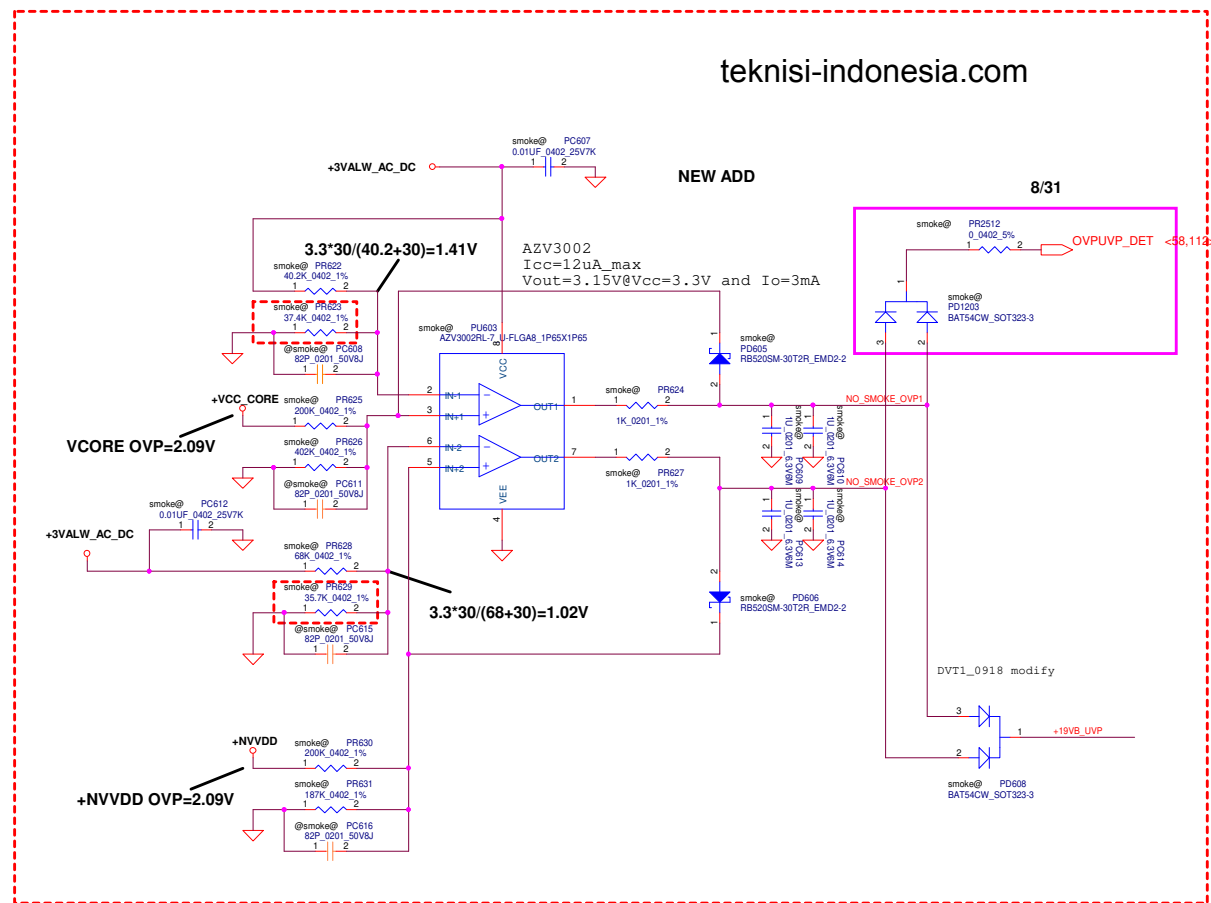
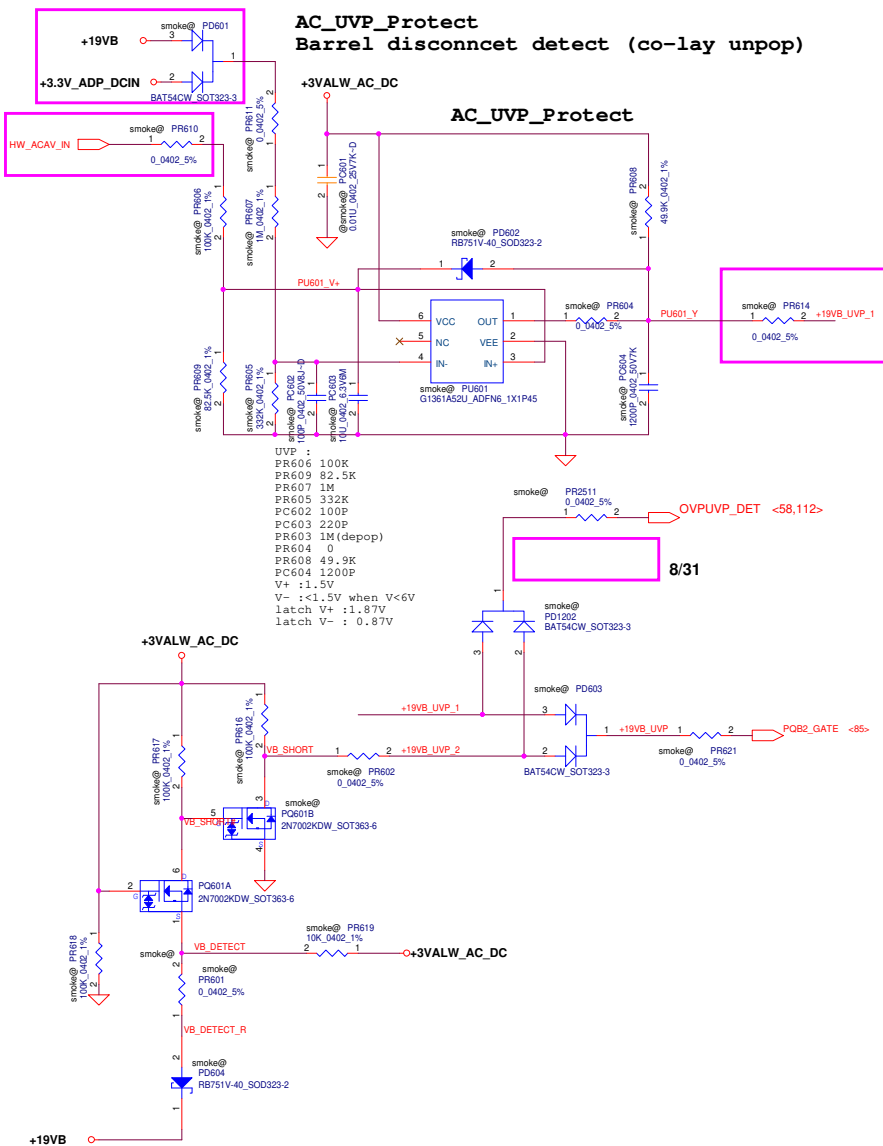
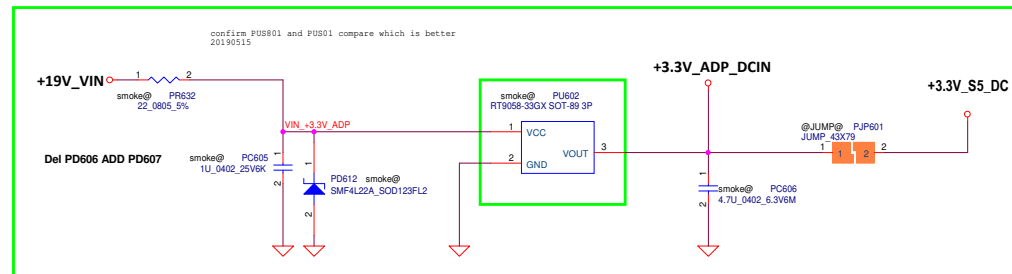
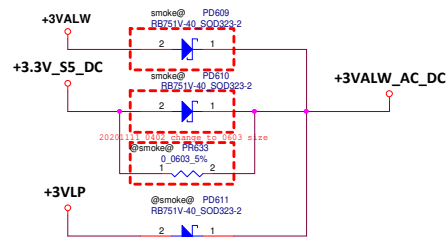


EN high: > VIN pin\* 0.7  
EN Low: < VIN pin\* 0.3



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**Main Func = Smokeless UVP**



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1	108	PWR_GPU_VRAM (UP9529)	8/13	PWR	change low voltage Mos	PQW1 change from SB00000EO00 to SB00001FN00	X00
2	112	PWR_Smokeless UVP/OVP	8/13	PWR	Add reserve resistor	Add 0 ohm resistor (SD028000080) bypass use	X00
3	82	PWR_DCIN / BATT CONN / OTP	9/15	PWR	DCIN pin define reverse	DCIN pin define reverse	X01
4	85	PWR_CHARGER (ISL95522A)	9/15	PWR	Add Current ability	Mount PQB12 and PQB14	X01
5	97	PWR_CPU CORE IC	9/16	PWR	Dell Dean request modify	PRZ64 change pull high to +Vccstg	X01
6	104	PWR_GPU_CORE SW (NCP303152)	9/17	PWR	Remove reserve reisitor	Remove PRV149、PRV151、PRV153、PRV155	X01
7	112	PWR_Smokeless UVP/OVP	11/11	PWR	PR633 0402 change to 0603	PR633 0402 change to 0603 (SD013000080)	X02
8	98	PWR_CPU_CORE_SW	11/12	PWR	Add 1pcs reserve 0603 MLCC in Vccsa power rail	Add PCA9 location	X02
9	82	PWR_DCIN / BATT CONN / OTP	11/12	PWR	+3.3V_ADAP_DCIN change to +3VLP	+3.3V_ADAP_DCIN change to +3VLP	X02
10	82	PWR_DCIN / BATT CONN / OTP	12/4	PWR	PR12 change to 1Mohm	PR12 from 10Mohm(SD000011M00) change to 1Mohm (SD034100480)	X03
11	112	PWR_Smokeless UVP/OVP	12/4	PWR	PR619 change to 1Kohm	PR619 from 10Kohm(SD034100280) change to 1Kohm (SD034100180)	X03
12							
							X01
							X01
							X01
							X01

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4				EMI			X01
5				PWR			X01
6				PWR			X01
7							X01
8							X01
9				PWR			X01
10				PWR			X01

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